

# TABLE OF CONTENTS

## MB

P01 : COVER SHEET  
P02 : SYSTEM BLOCK DIAGRAM  
P03 : POWER MAP  
P04 : POWER SEQUENCY DIAGRAM  
P05 : CLOCK MAP  
P06 : SMBUS&I2C MAP  
P07 : POWER SEQUENCE  
P08 : DCIN/BATT  
P09 : PWR\_CHARGE  
P10 : PWR\_5V/3.3V  
P11 : PWR\_VTT  
P12 : PWR\_1.5V/0.75S  
P13 : PWR\_CPU\_VCORE  
P14 : PWR\_OTHER  
P15 : PWR\_(Empty)  
P16 : PWR\_1.8VS  
P17 : PWR\_(Empty)  
P18 : POWER SEQUENCY CHART  
P19 : Penryn(HOST BUS)1/3  
P20 : Penryn(HOST BUS)2/3  
P21 : Penryn(Power/Gnd)3/3  
P22 : Cantiga (HOST) 1/7  
P23 : Cantiga (DMI) 2/7

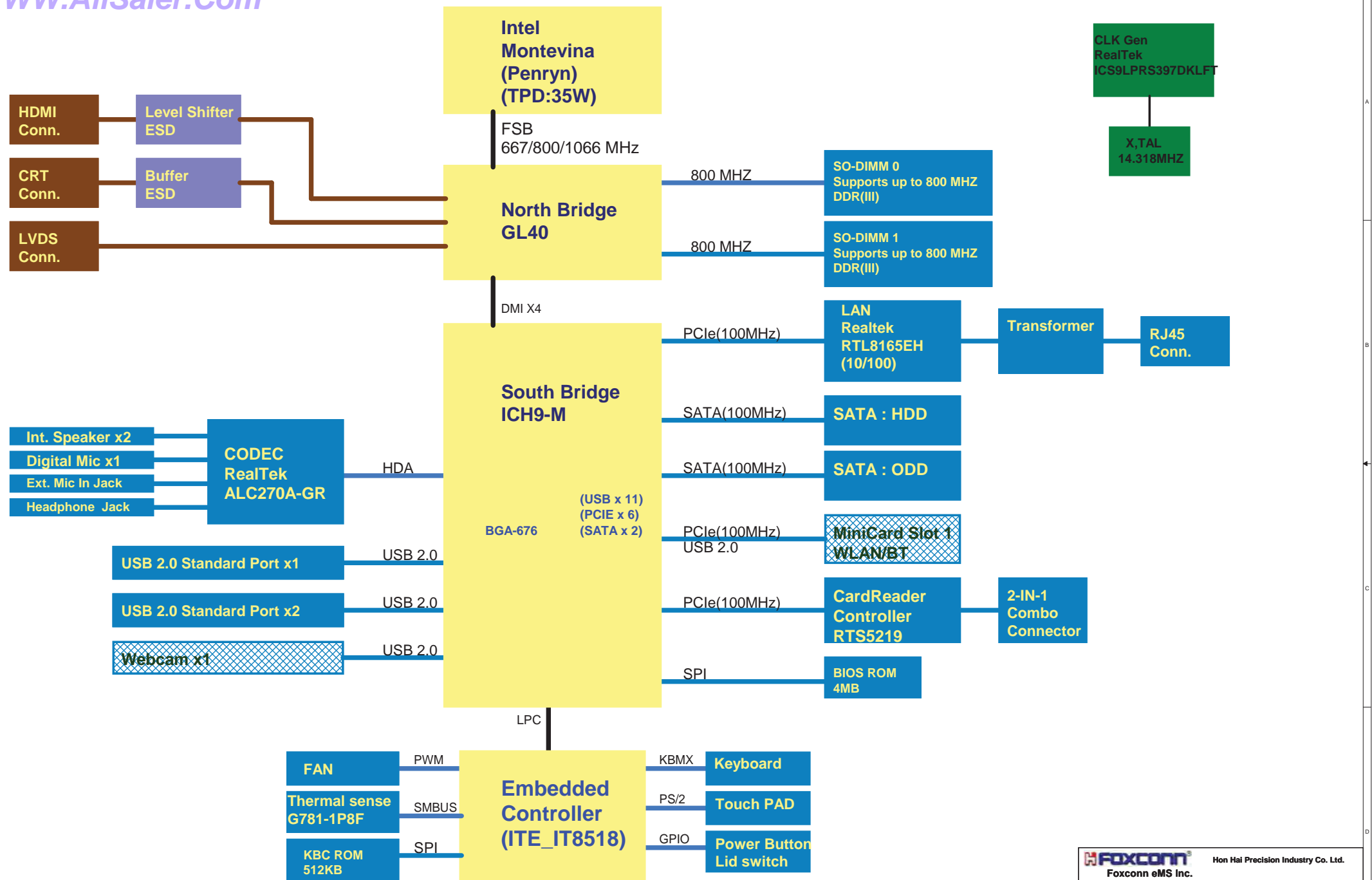
P24 : Cantiga (GRAPHIC) 3/7  
P25 : Cantiga (DDR3) 4/7  
P26 : Cantiga (POWER,VCC) 5/7  
P27 : Cantiga (VCC CORE) 6/7  
P28 : Cantiga (VSS) 7/7  
P29 : ICH9-M (PCI/USB) 1/5  
P30 : ICH9-M(LPC,IDE,SATA) 2/5  
P31 : ICH9-M (GPIO) 3/5  
P32 : ICH9-M (POWER) 4/5  
P33 : ICH9-M (GND) 5/5  
P34 : DDR3(SO-DIMM\_0) 1/2  
P35 : DDR3(SO-DIMM\_1) 2/2  
P36 : CLOCK GEN  
P37 : EC+KBC (IT8518)  
P38 : Audio(CODEC)  
P39 : Audio(JACK/SPEAKER/MIC)  
P40 : LAN (RTL8165EH)  
P41 : Card Reader(RTL5219)  
P42 : Mini PCIe&BT/PWRB/Control  
P43 : USBX2/USB DB/SATA CONN  
P44 : LVDS/Webcam  
P45 : HDMI & CRT  
P46 : Thermal/Fan/Stitch Cap

P. Leader	Check by	Design by

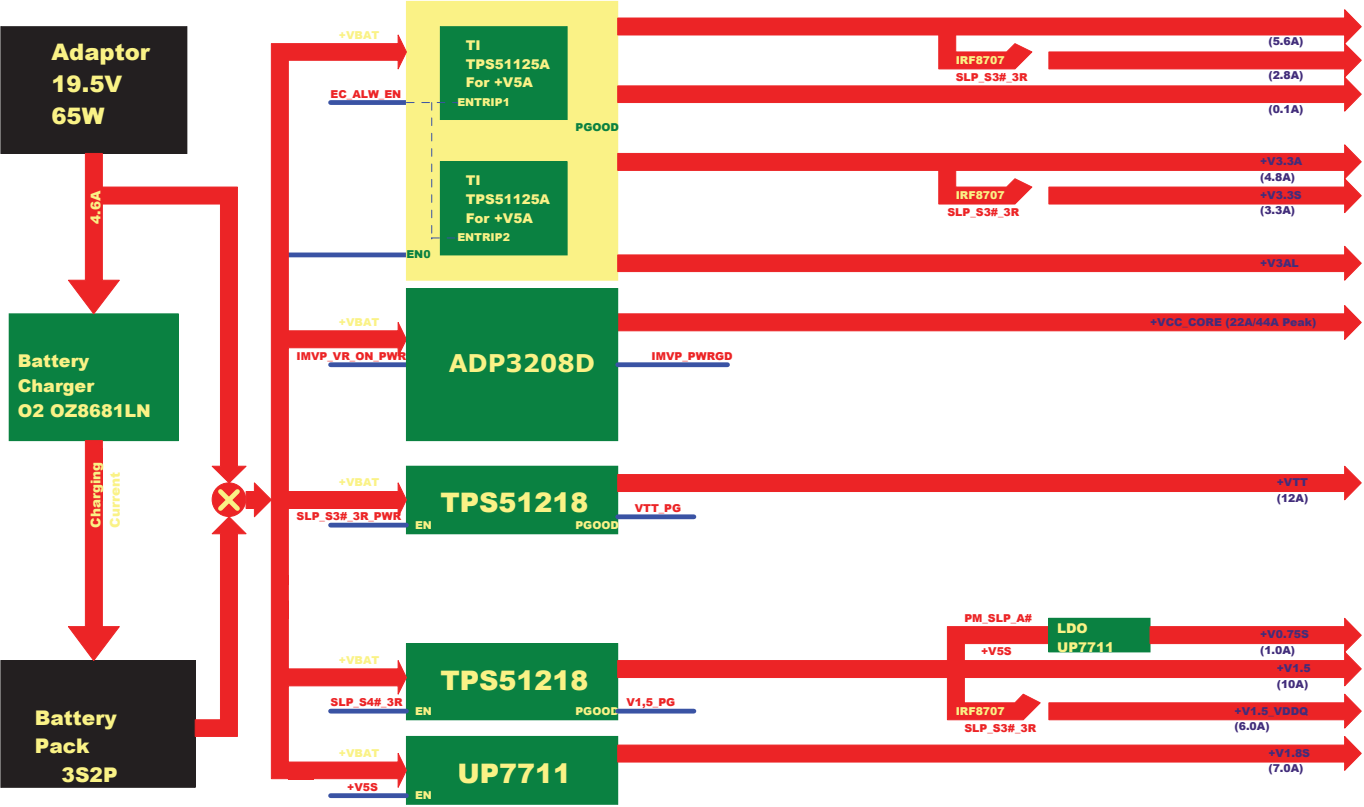
**Foxconn**  
**Foxconn eMS Inc.**  
HNBD R&D

Hon Hai Precision Industry Co. Ltd.  
phone: +886-2-2799-6111

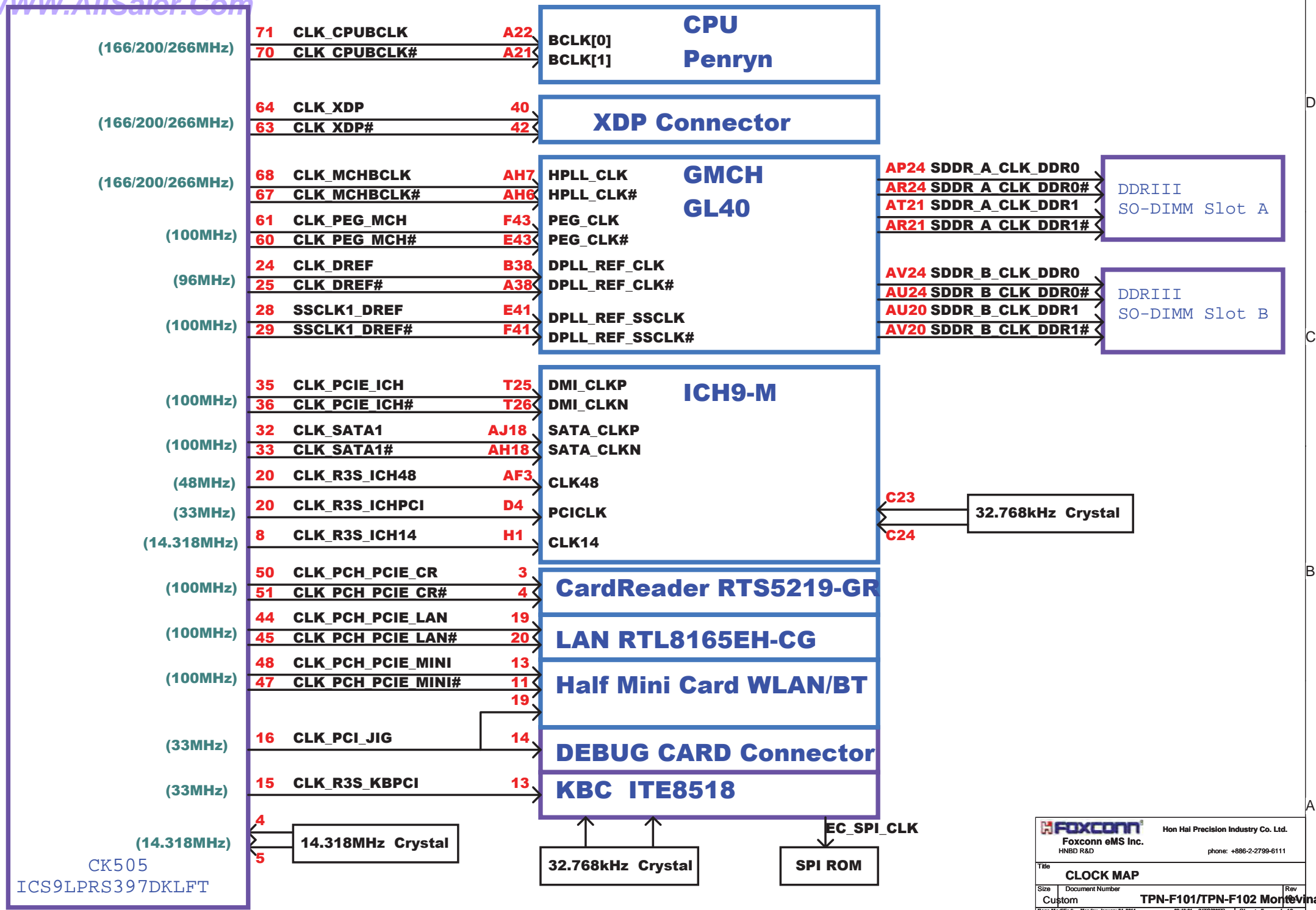
Title		
Index Page		
Size	Document Number	Rev
Custom	TPN-F101/TPN-F102 Montevina	
Page Modified: Monday, January 24, 2011 08:43:01 (UTC/GMT) Sheet 1 of 46		

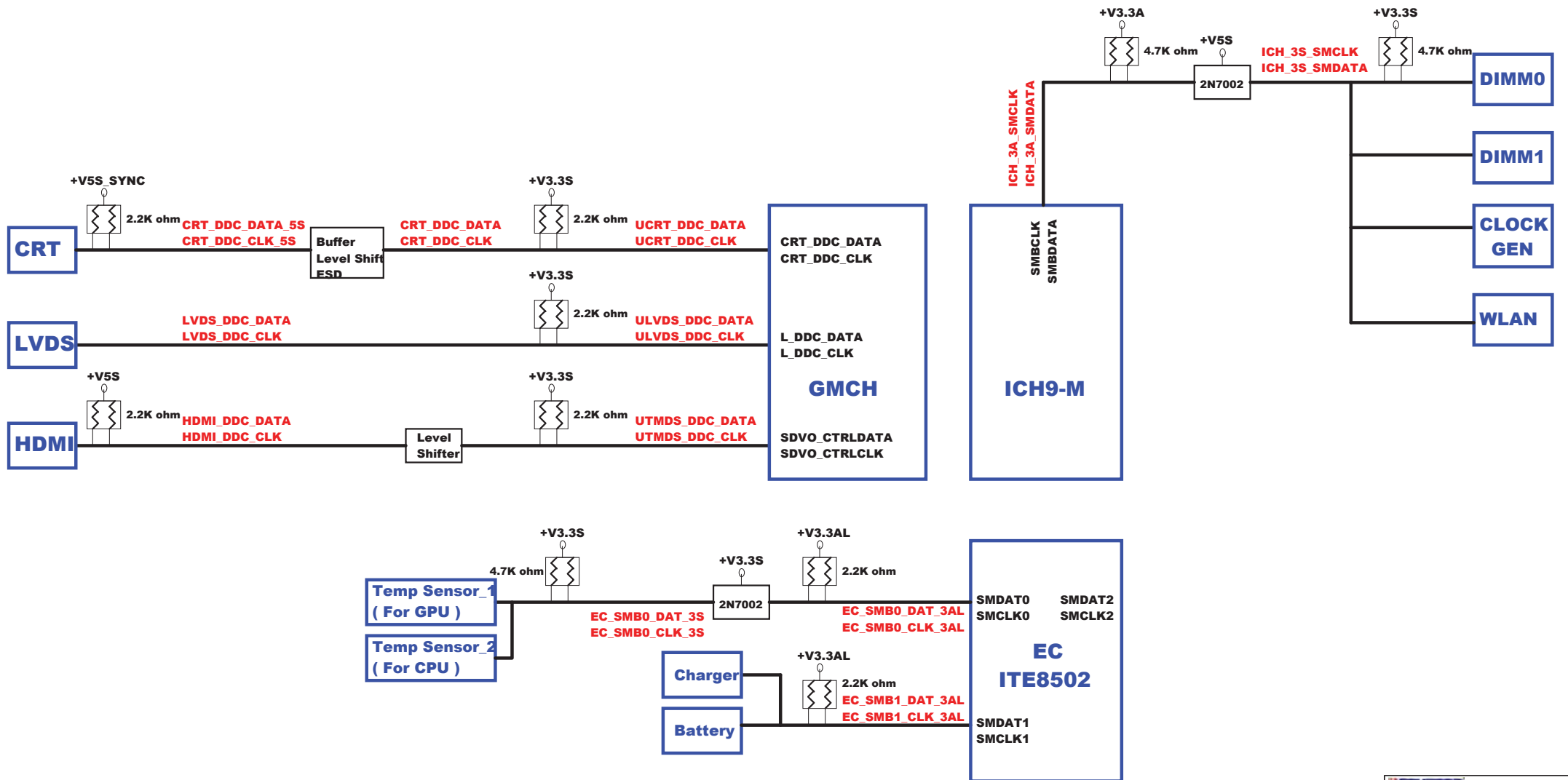


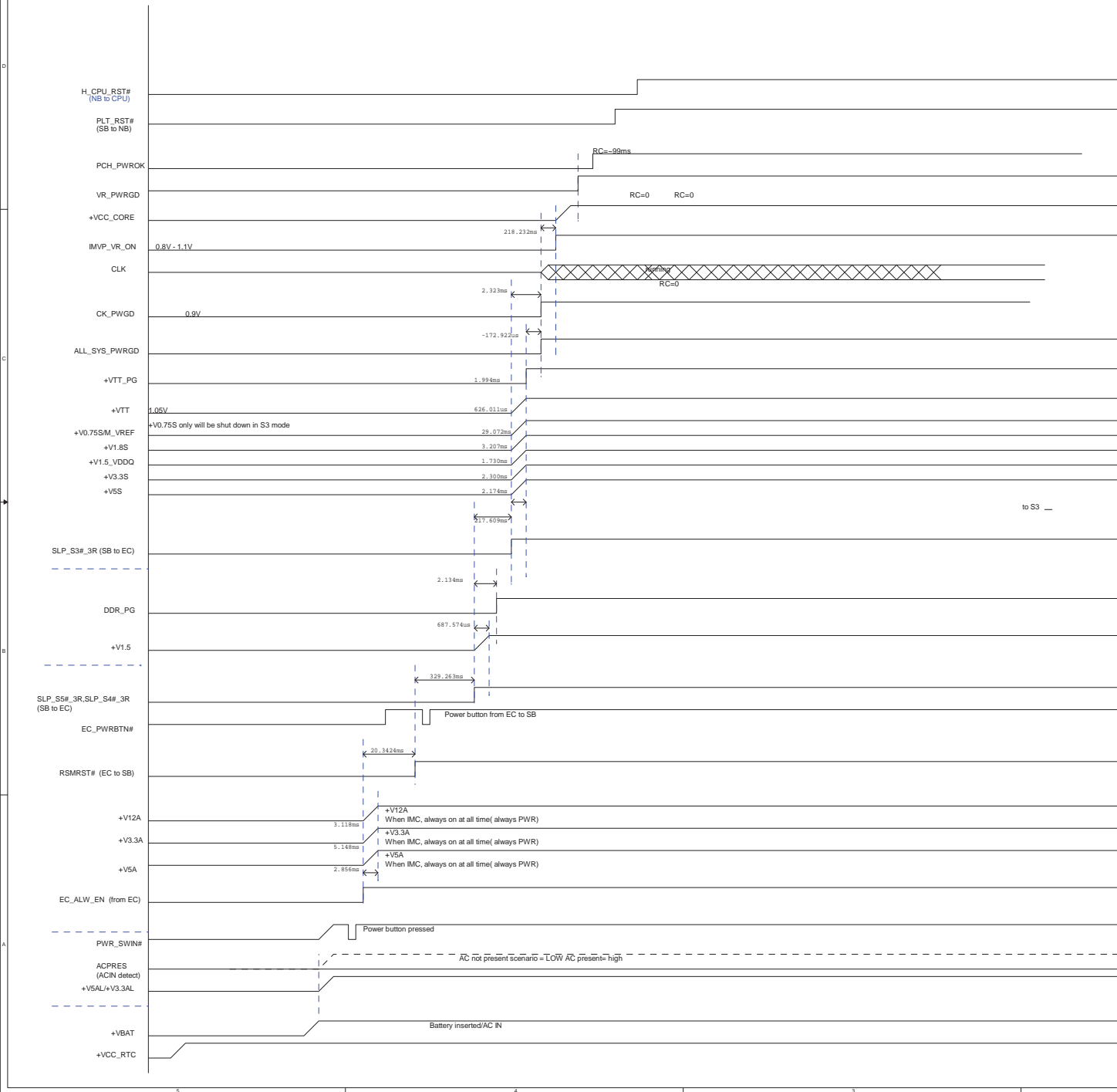
POWER MAP











Power on Sequence required:

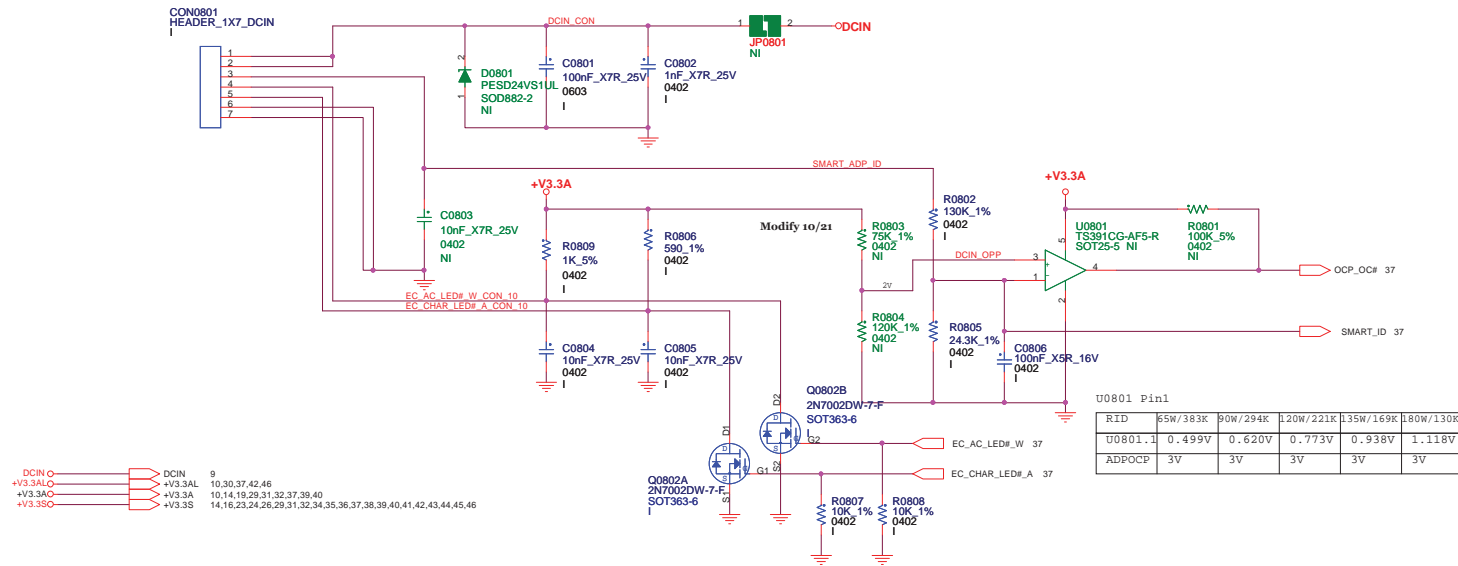
ICH9M:

- 1, +V3.3A ramp before +V1.1A
- 2, +V3.3S ramp before +V1.8S
- 3, +V1.8S ramp before +V1.1S
- 5, +V3.3A ramping down time > 300us
- 6, 50uS <= All power rails except +V3.3A <= 40mS
- 7, 100uS <= +V3.3A <= 40mS

GMCH:

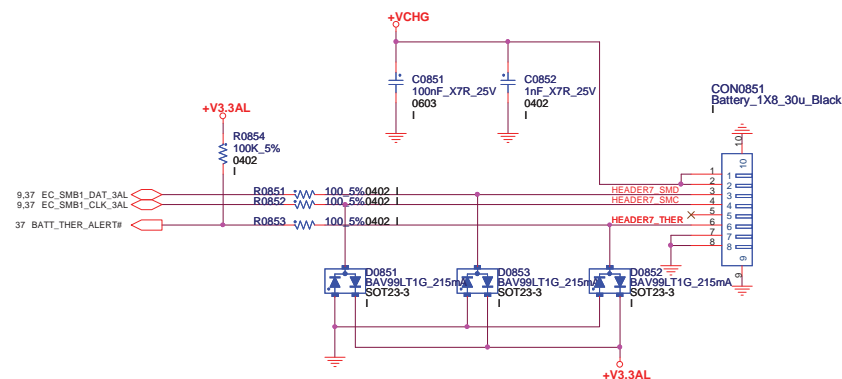
- 1, 0 < (+V3.3S) - (+V1.8S) < 2.1
- 2, +V1.8S ramp before +V1.1S
- 3, +V1.1S ramp before +VCC\_NB

# DC\_JACK WIRE to BOARD CONNECTOR



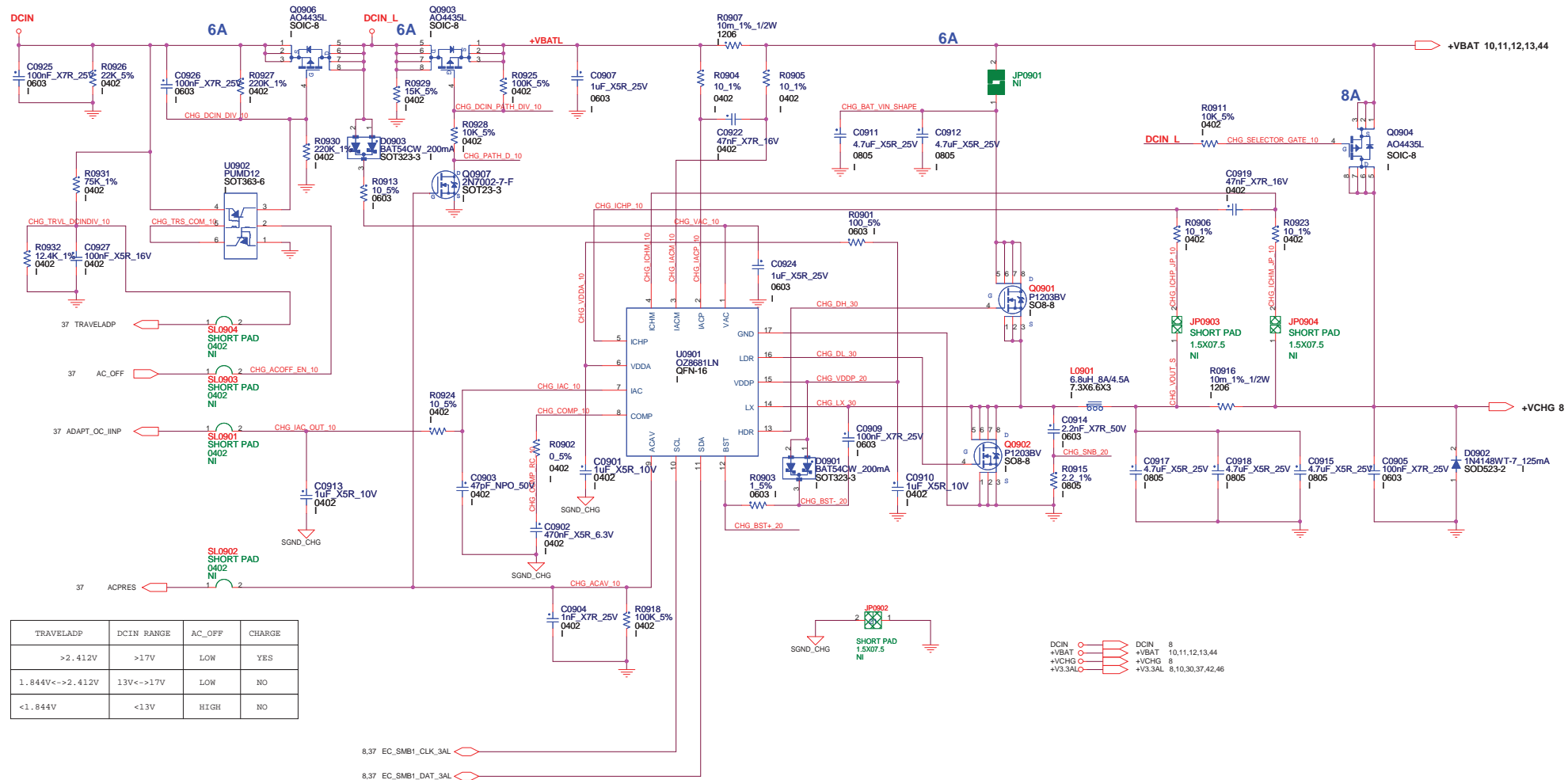
# BATTERY CONNECTOR

2010.0914.0





# BATTERY CHARGER

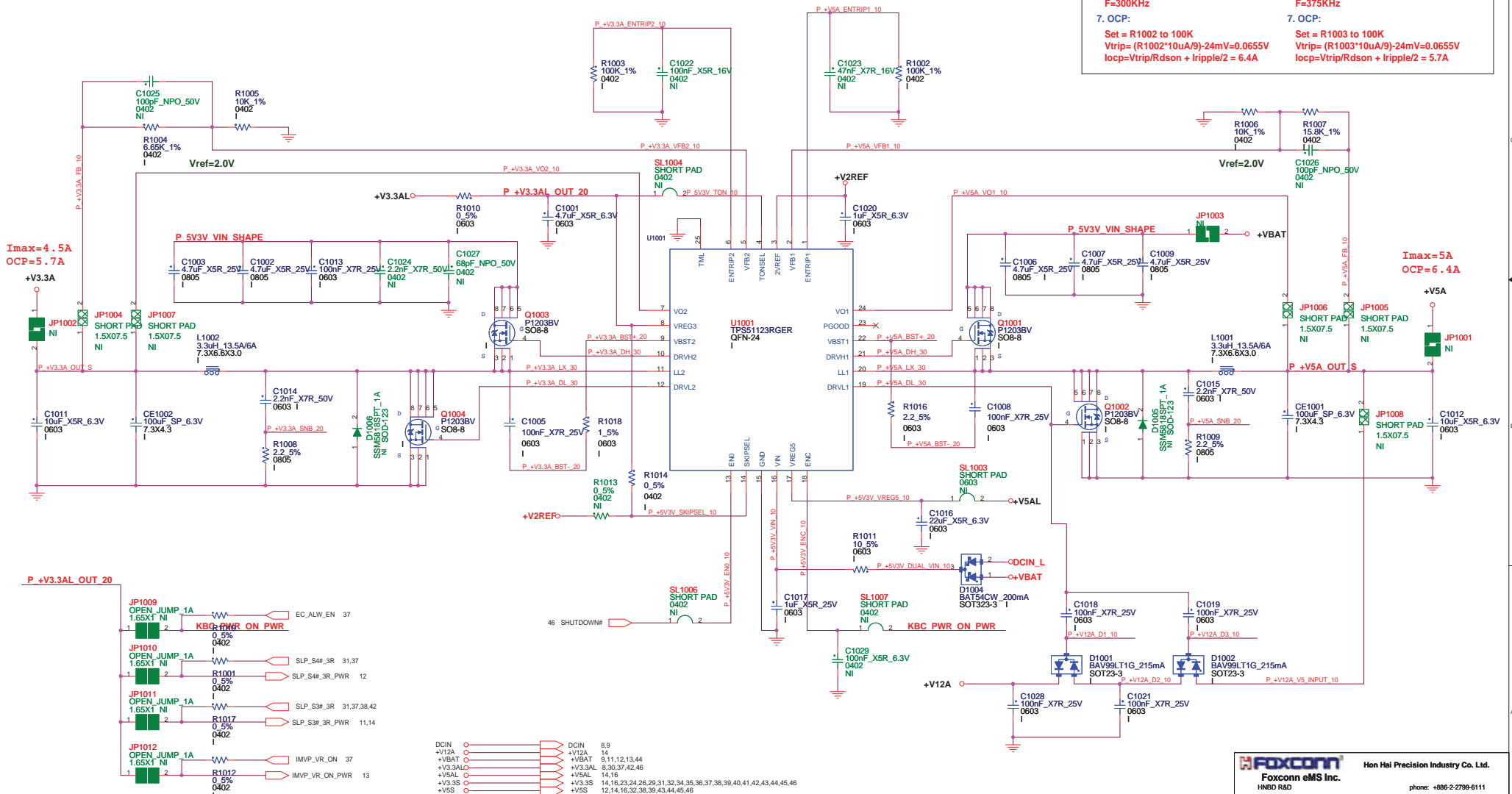


TRAVELADP	DCIN RANGE	AC_OFF	CHARGE
>2.412V	>17V	LOW	YES
1.844V<->2.412V	13V<->17V	LOW	NO
<1.844V	<13V	HIGH	NO

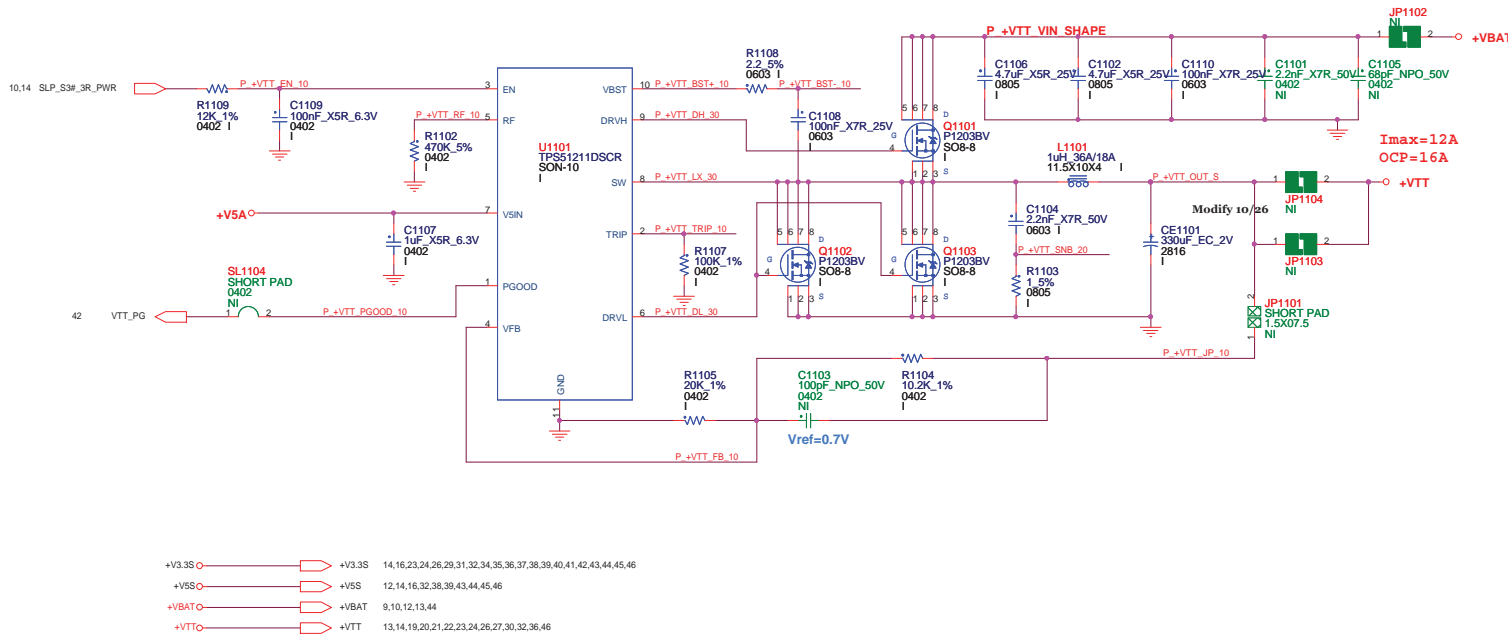
# +V5A / +V3.3A POWER SUPPLY

2010.1103.0

<b>+V5A:</b> 1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 3.7A$ 2. Ripple Current: $I_{rip} = 3.72A$ 3. Ripple Voltage: $ESR/1 = 15mohm$ $V_{rip} = 55.8mV$ 4. Inductor Spec: $I_{sat} = 13.5A$ $I_{dc} = 6A$ $DCR = 30mohm$ 5. MOSFET Spec: H-side MOSFET: IRF8707PBF $R_{ds(ON)} = 17.5mohm$ ( $V_{gs} = 4.5V$ ) $I_{cont} = 11A$ ( $T = 25^{\circ}C$ ) $I_{peak} = 88A$ (Pause $\geq 10us$ ) 6. Frequency: $F = 300KHz$ 7. OCP: $Set = R1002$ to 100K $V_{trip} = (R1002 \cdot 10uA/9) - 24mV = 0.0655V$ $I_{ocp} = V_{trip} / R_{dson} + I_{ripple} / 2 = 6.4A$	<b>+V3.3A:</b> 1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 2.2A$ 2. Ripple Current: $I_{rip} = 2.21A$ 3. Ripple Voltage: $ESR/1 = 15mohm$ $V_{rip} = 33.15mV$ 4. Inductor Spec: $I_{sat} = 13.5A$ $I_{dc} = 6A$ $DCR = 30mohm$ 5. MOSFET Spec: L-side MOSFET: IRF8707PBF $R_{ds(ON)} = 17.5mohm$ ( $V_{gs} = 4.5V$ ) $I_{cont} = 11A$ ( $T = 25^{\circ}C$ ) $I_{peak} = 88A$ (Pause $\geq 10us$ ) 6. Frequency: $F = 375KHz$ 7. OCP: $Set = R1003$ to 100K $V_{trip} = (R1003 \cdot 10uA/9) - 24mV = 0.0655V$ $I_{ocp} = V_{trip} / R_{dson} + I_{ripple} / 2 = 5.7A$
--	---

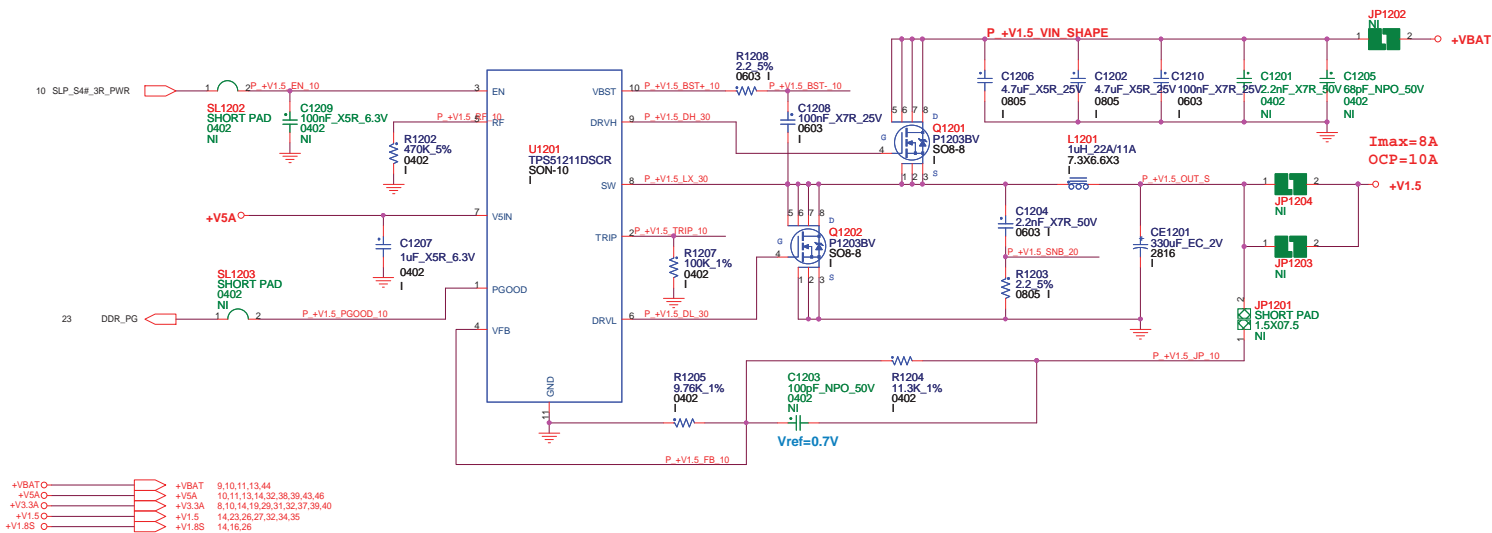


## +VTT POWER SUPPLY

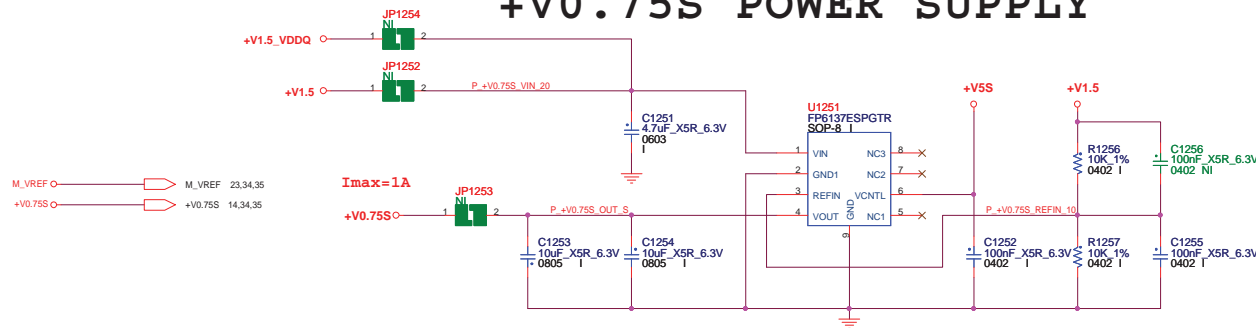


- +VTT:**
- I/P Current:**  
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.86A$
  - Ripple Current:**  
 $I_{rip} = 3.42A$
  - Ripple Voltage:**  
 $ESR/1 = 9m\Omega$   
 $V_{rip} = 30.78mV$
  - Inductor Spec:**  
 $I_{sat} = 36A$   
 $I_{dc} = 18A$   
 $DCR = 3.3m\Omega$
  - MOSFET Spec:**  
**H-side MOSFET: IRF8707PBF**  
 $R_{ds(ON)} = 17.5m\Omega$  ( $V_{gs} = 4.5V$ )  
 $I_{cont} = 11A$  ( $T = 25^\circ C$ )  
 $I_{peak} = 88A$  (Pause = 10 us)  
**L-side MOSFET: IRF8707PBF**  
 $R_{ds(ON)} = 17.5m\Omega$  ( $V_{gs} = 4.5V$ )  
 $I_{cont} = 11A$  ( $T = 25^\circ C$ )  
 $I_{peak} = 88A$  (Pause = 10 us)
  - Frequency:**  
 $F = 290KHz$  ( $R_{0802} = 470K$ )
  - OCP:**  
 $Set = R_{0807} \text{ to } 100K$   
 $V_{trips} = R_{0807} \cdot I_o = 1V$   
 $I_{ocp} = (V_{trips} / 8 \cdot R_{ds(on)}) + I_{ripple} / 2 = 16A$

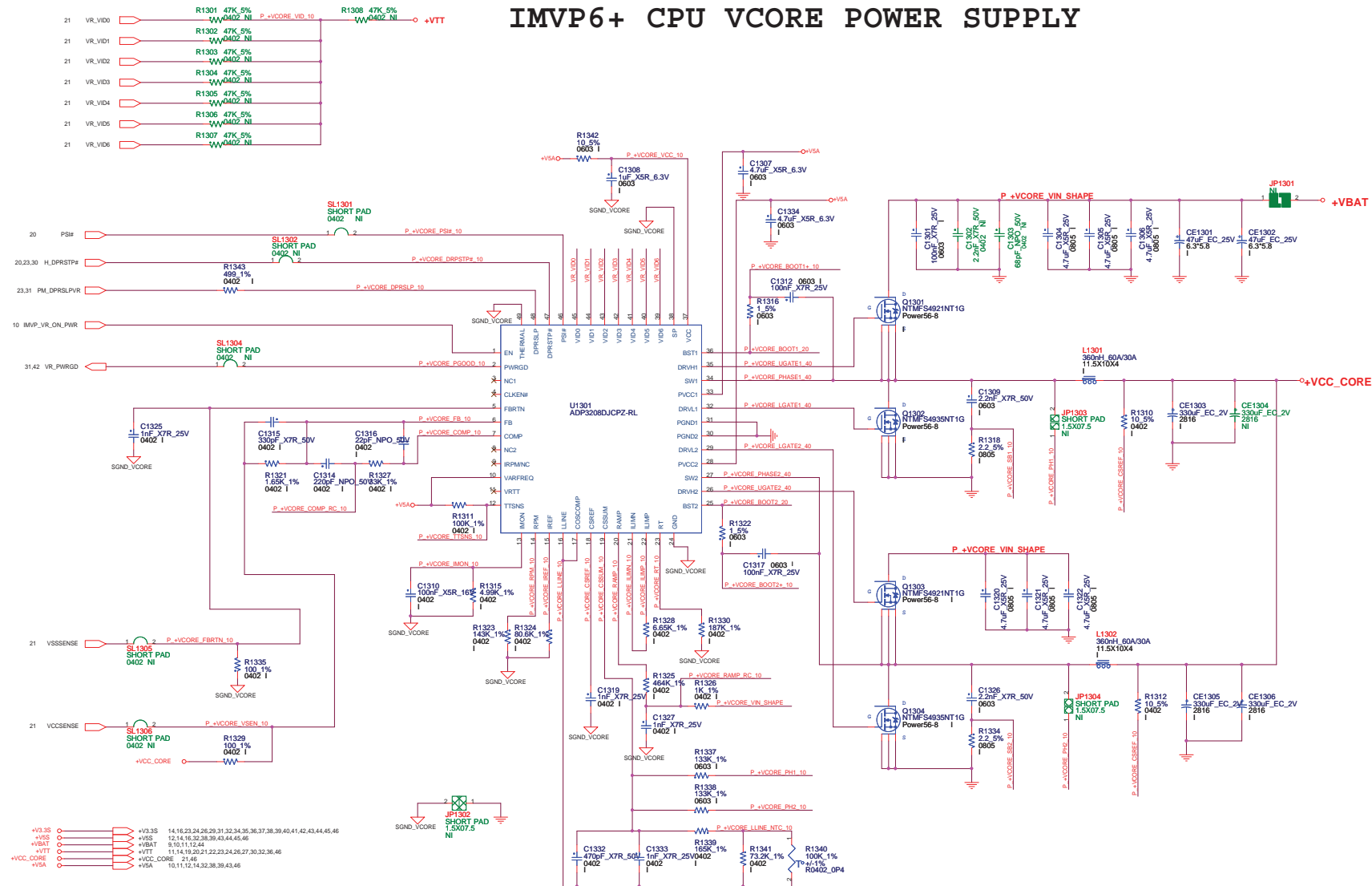
## +V1.5 POWER SUPPLY



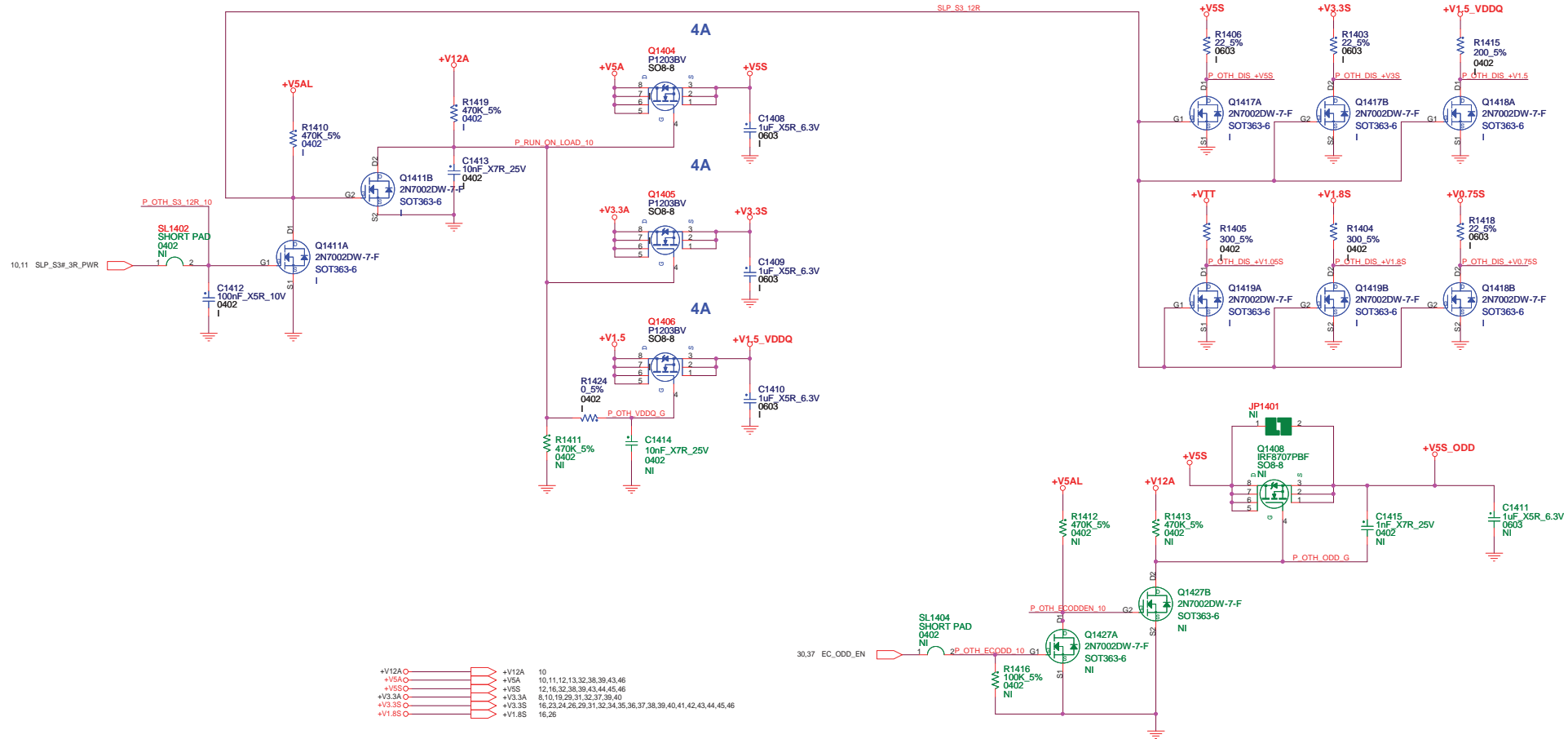
## +V0.75S POWER SUPPLY



# IMVP6+ CPU VCORE POWER SUPPLY

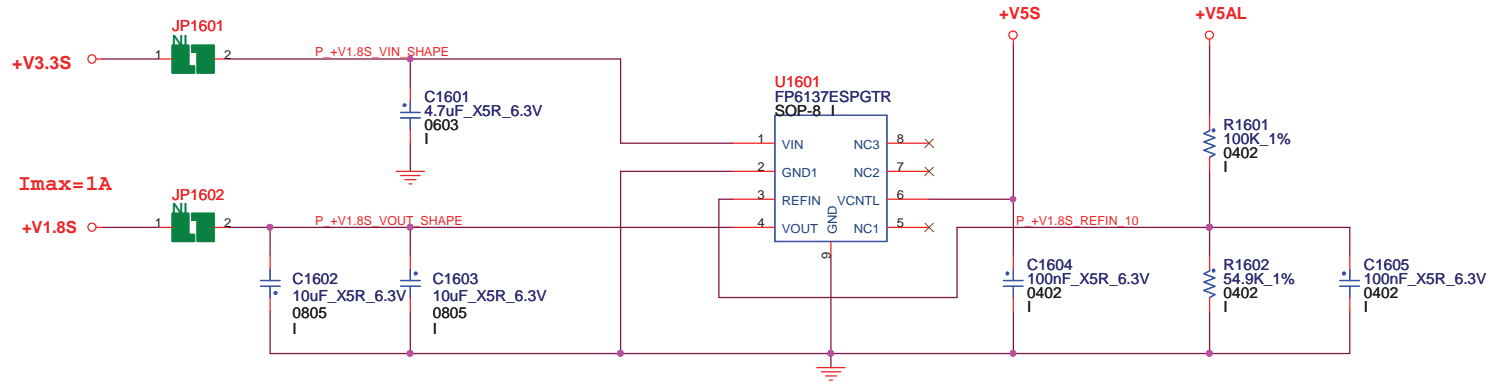


# OTHER POWER / DISCHARGE CIRCUITS





# +V1.8S POWER SUPPLY



<b>FOXCONN</b> <b>Foxconn eMS Inc.</b> 8807 Fallbrook Drive HNBD R&D		Hon Hai Precision Industry Co. Ltd. phone: +886-2-2799-6111 fax: (281) 668-1515	
Title		PWR_1.8VS	
Size	Document Number		Rev
Customer	CHICAGO		0.1
Page Modified: Monday, January 24, 2011		08:43:02 (UTC/GMT)	Sheet 16 of 46





Signals	Test Point
LDT_RST#	CX61
LDT_PG	RX23
CPU_CLKIN	CX72 ; CX73
NB_PWRGD	RX30
SB_PWRGD	DS63
+VCC_NB	PJ21/2
+VLDT	PJP15/2
+V1.1S	PJP15/1
VRM_PWRGD	DB7/2
+VDDR_CPU	PJ16/1
+VCC_CORE	PCE12
+VDDNB_CPU	PJ17/2
VDDA_PWRGD	PR211
+VDDA_CPU	PJ22/2
+V1.5S	PJ28/1
V1.8S_PWRGD	DS7/1
+V1.8S	PJ2/1
+V3.3S	PC170
+V5S	PC175
+V12S	PQ41/D
SLP_S3M_3R	RS60
+V0.75S	PJ8/2
M_VREF	PC182
+V1.5	RS76
SLP_S5M_3R	DB/2
EC_PWRBTN#	RS61
RSMRST#	PJ23/2
+V1.1A	PC109
+V3.3A	PJ25
+V5A	PC169
+V12A	PQ27/G
EC_ALW_EN	HEADER2/B
PWR_SWIN#	RS51
ACPRES	PC164
+V5AL	PJ24
+V3.3AL	PC61
M31ALDO	PJ19/2
+VBAT	CS48
+VCC_RTC	

CPU MEM CTL & DDR3 SODIMM PWR#

SLP\_S5M\_3R, SLP\_S4M\_3R (SB to EC)

CPU\_TMM/SB/SB\_SCL1/2 SB\_XB/SP1/LPC ROM PWR#

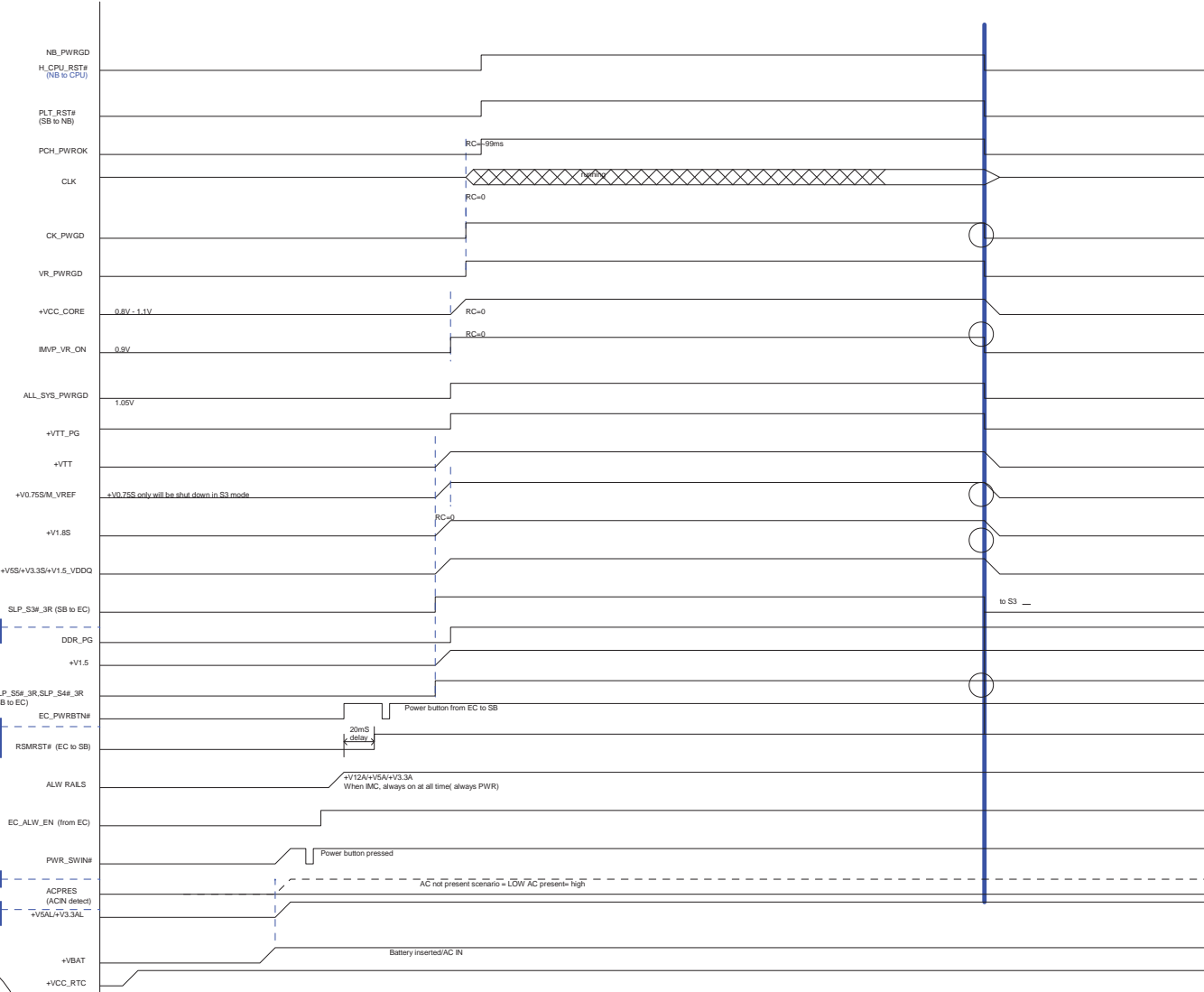
KBC is ready

KBC is powered by +V3.3AL

Power on Sequence required:

ICH9M:  
1. +V3.3A ramp before +V1.1A  
2. +V3.3S ramp before +V1.8S  
3. +V1.8S ramp before +V1.1S  
5. +V3.3A ramping down time > 300us  
6. 50us <= All power rails except +V3.3A <= 40ms  
7. 100us <= +V3.3A <= 40ms

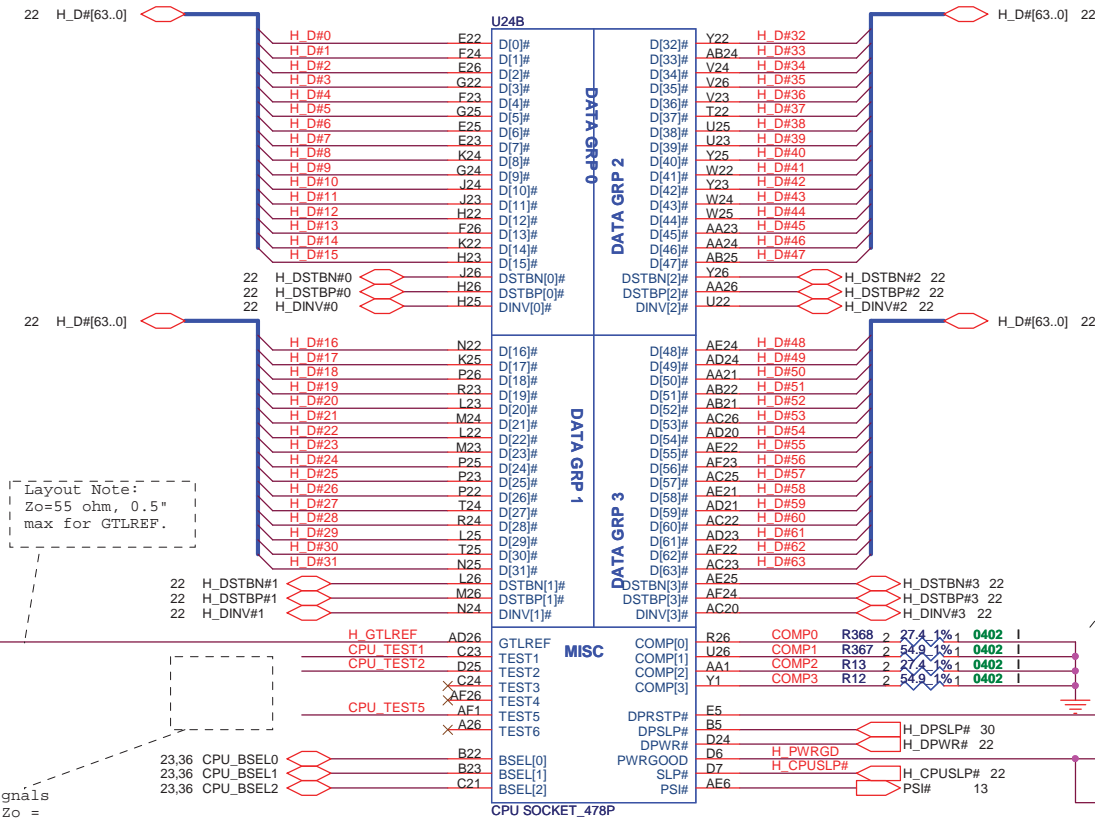
GMCH:  
1. 0 < (+V3.3S) - (+V1.8S) < 2.1  
2. +V1.8S ramp before +V1.1S  
3. +V1.1S ramp before +VCC\_NB



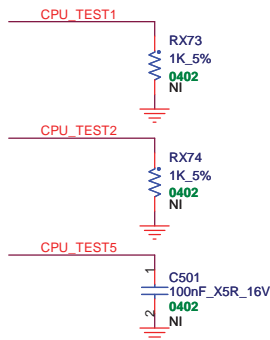


Place close to CPU

Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection. TEST4 and TEST6 and TEST7 pins can be left NC.

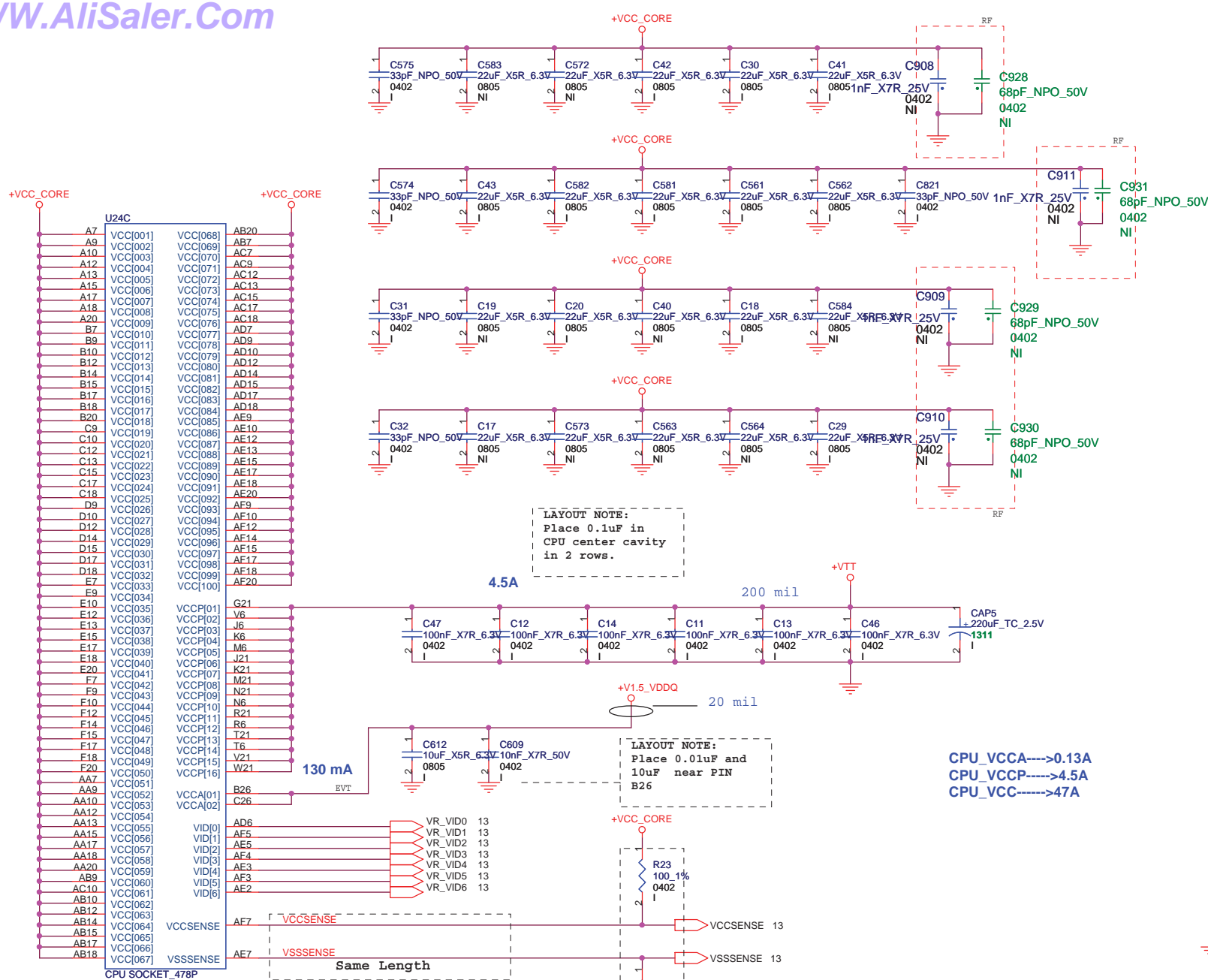


Layout Note:  
Comp0,2 connect with Zo=27.4 ohm, make trace length shorter then 0.5". Width=18mil(MS)  
Comp1,3 connect with Zo=55 ohm, make trace length shorter then 0.5". Width=5mil(MS)



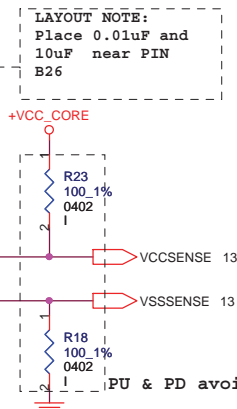
**Foxconn**  
Foxconn eMS Inc.  
HNBD R&D  
Hon Hai Precision Industry Co. Ltd.  
phone: +886-2-2799-6111

Title		
Penryn (HOST BUS) 2/3		
Size	Document Number	Rev
Custom	TPN-F101/TPN-F102 Montevina	
Page Modified: Monday, January 24, 2011 09:05:38 (UTC/GMT) Sheet 20 of 46		

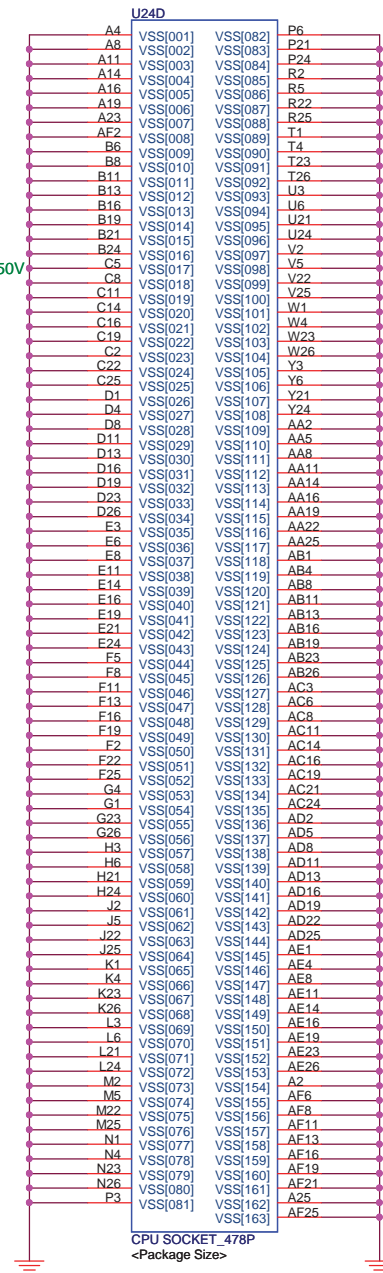


Outer width=18 mil spacing=7 mil  
Inner width=14 mil spacing=7 mil  
Length match < 25 mil

Layout Note: Route VCCSENSE & VSSSENSE traces at 27.4 Ohms with 25 mil spacing to other signals. Place PU and PD within 1 inch of CPU.



CPU\_VCCA---->0.13A  
CPU\_VCCP---->4.5A  
CPU\_VCC---->47A



Hon Hai Precision Industry Co. Ltd.

Foxconn EMS Inc.

HNBD R&D

phone: +886-2-2799-6111

Title

Penryn (POWER/GROUND) 3/3

Size

Document Number

Custom

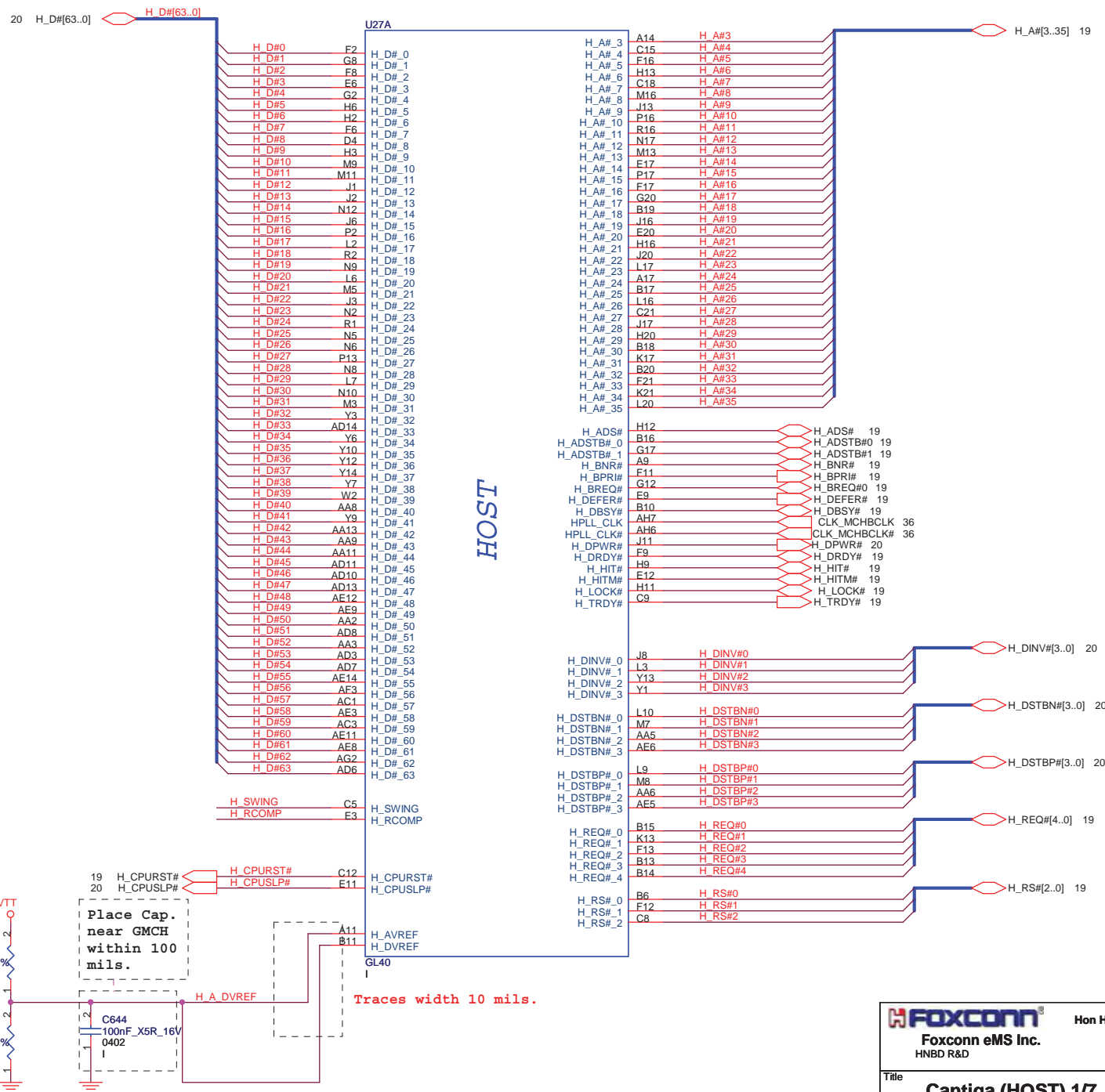
Page Modified: Monday, January 24, 2011

Rev

TPN-F101/TPN-F102 Montevina

08:55:39 (UTC/GMT)

Sheet 21 of 46

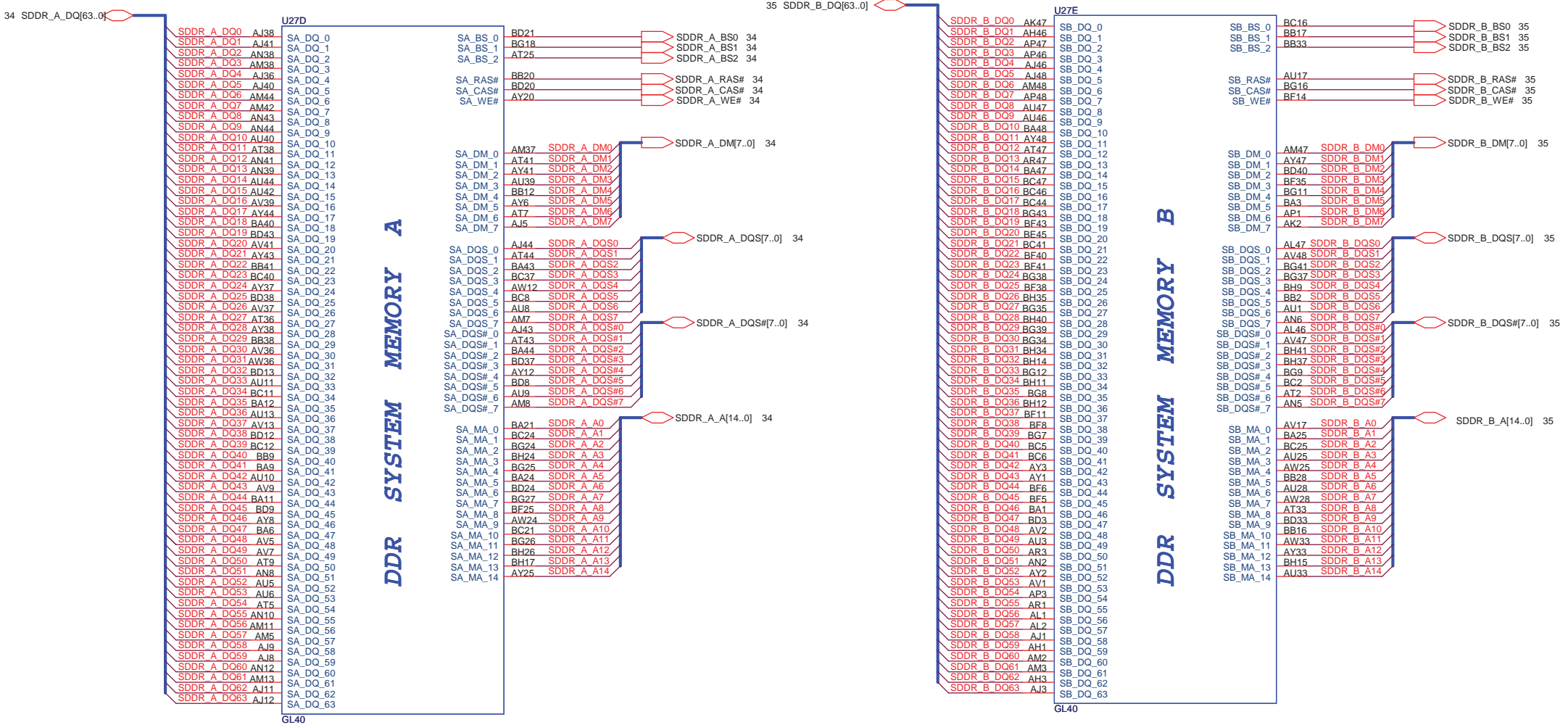


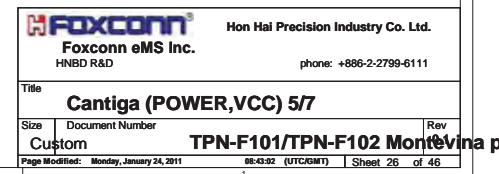


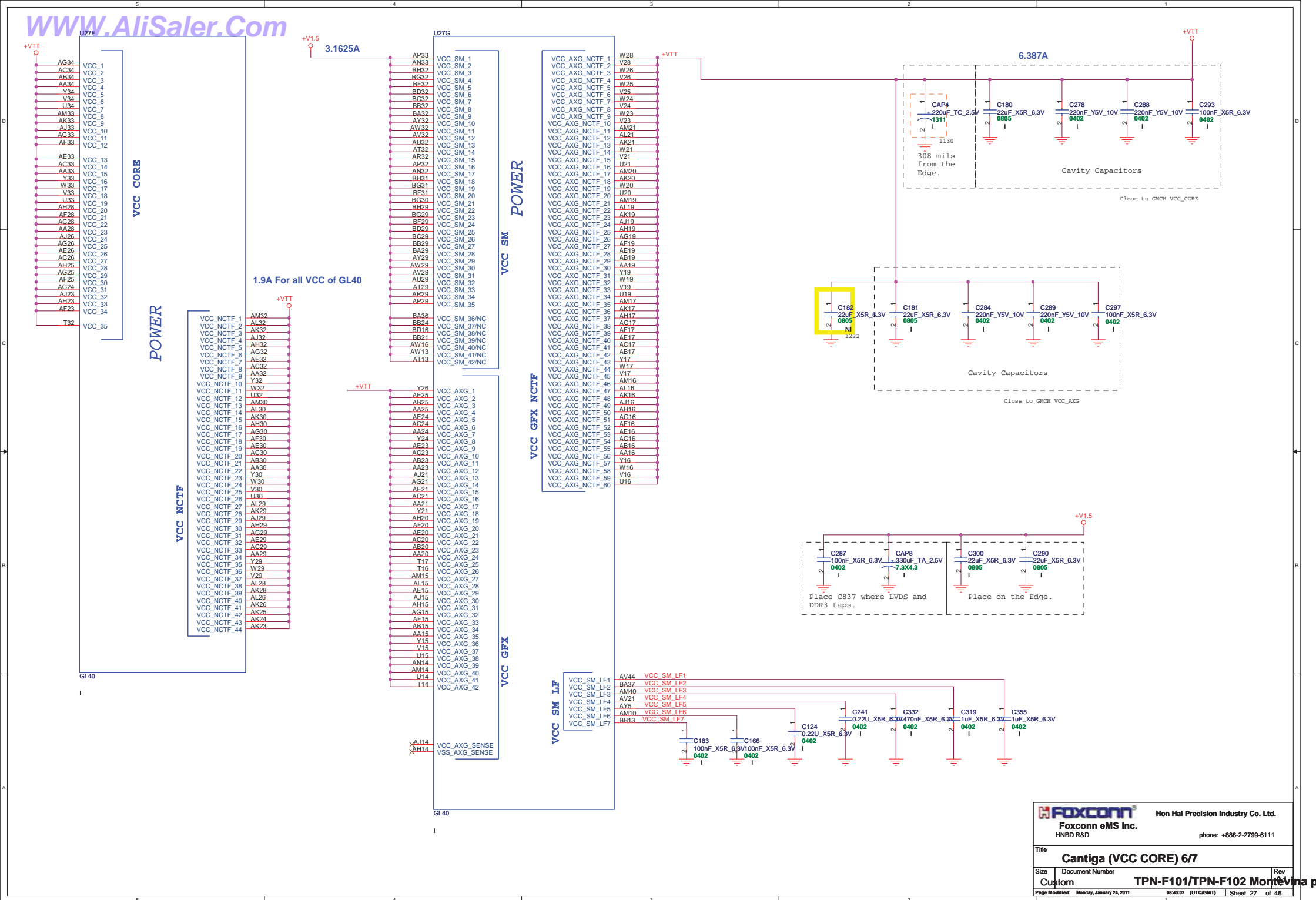


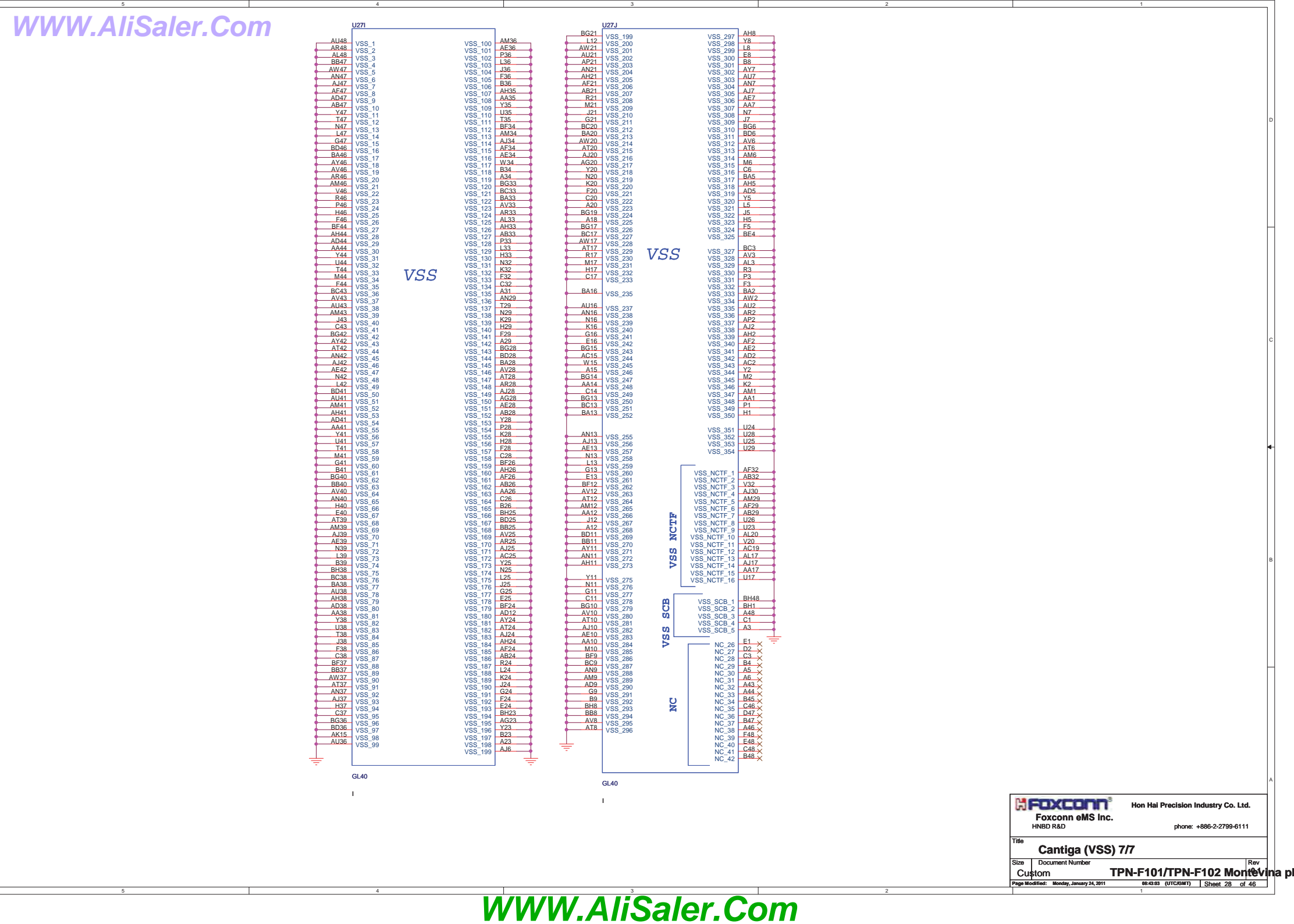


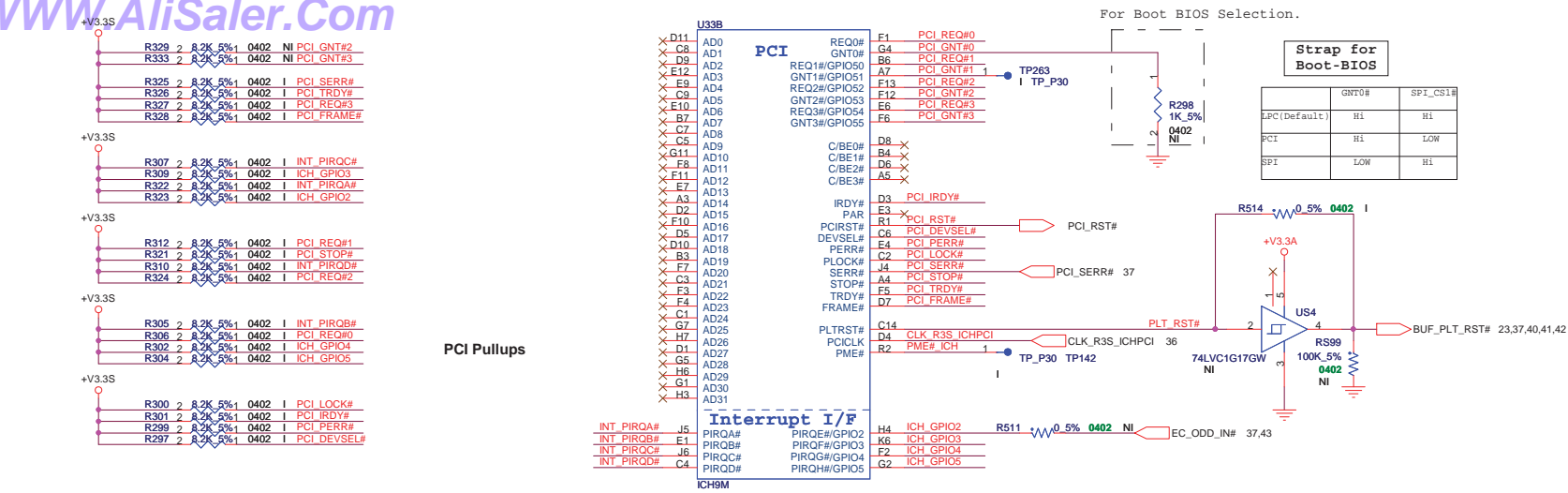




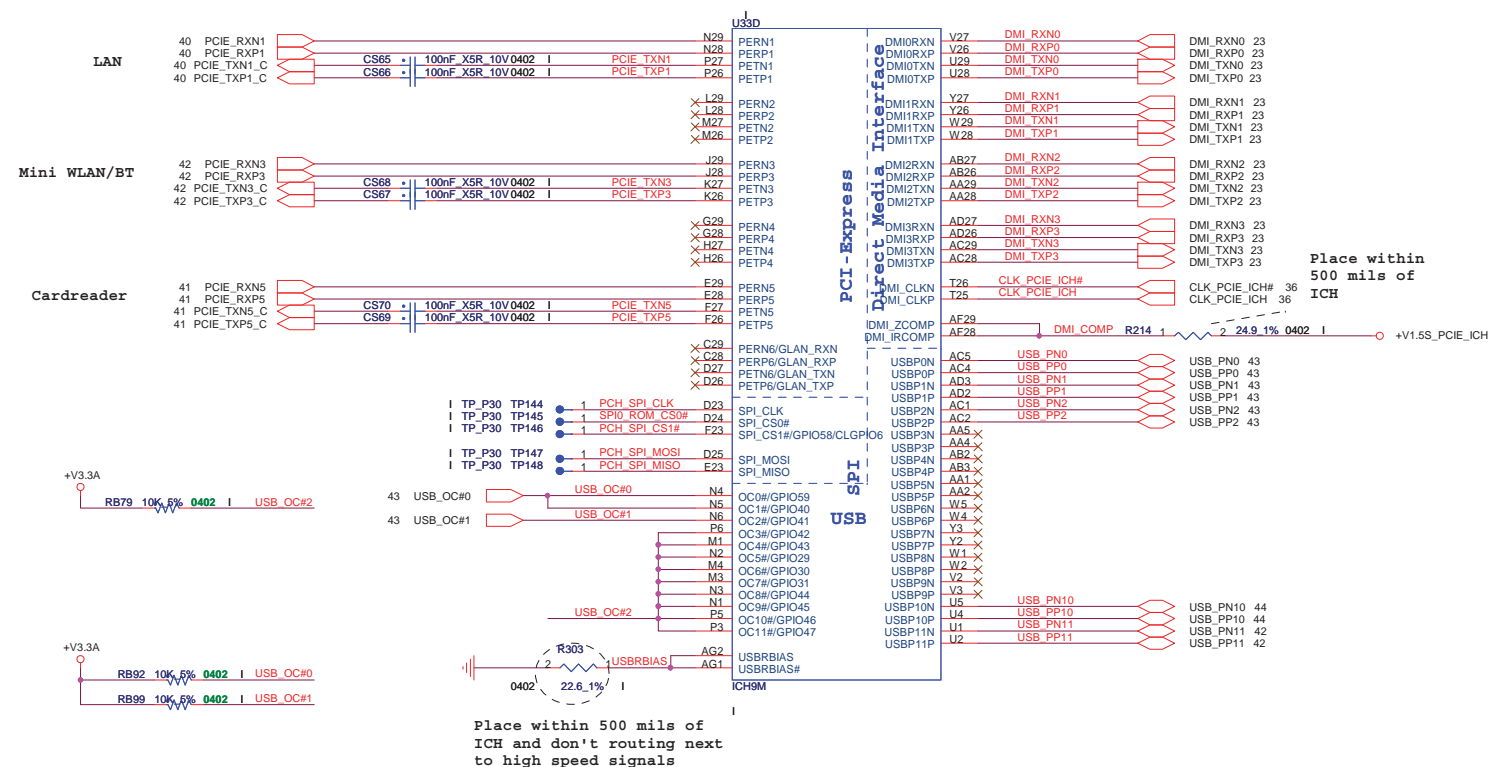


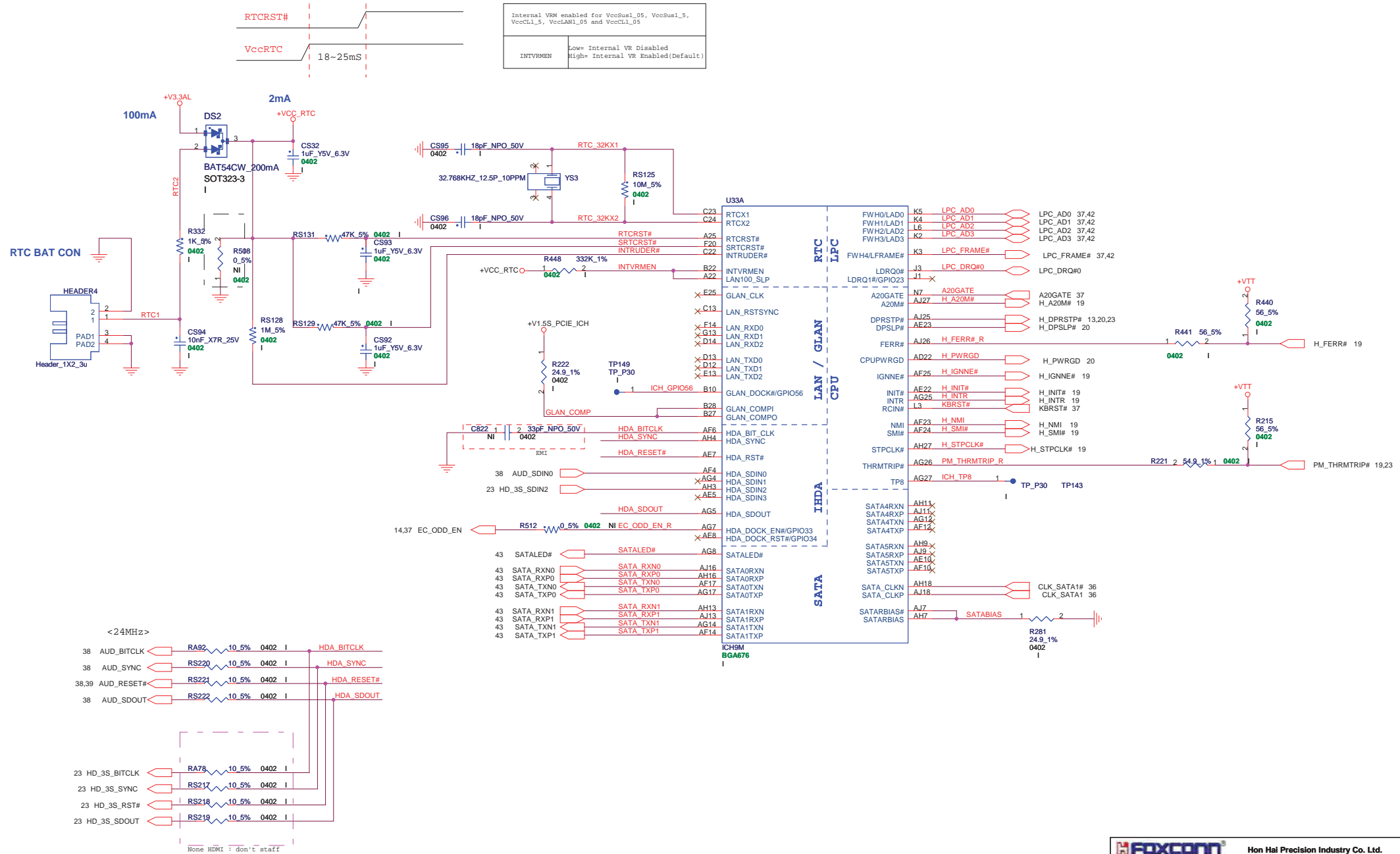




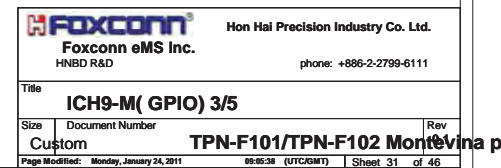


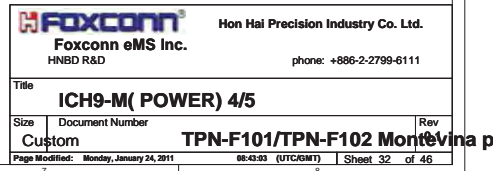
USB PORT	Function	OC pin
PORT-0	Ext. USB 0	
PORT-1	Ext. USB 1	
PORT-2	Ext. USB 2	
PORT-3		
PORT-4		
PORT-5		
PORT-6		
PORT-7		
PORT-8		
PORT-9		
PORT-10	Camera	
PORT-11	WLAN/BT	
PORT-12		
PORT-13		



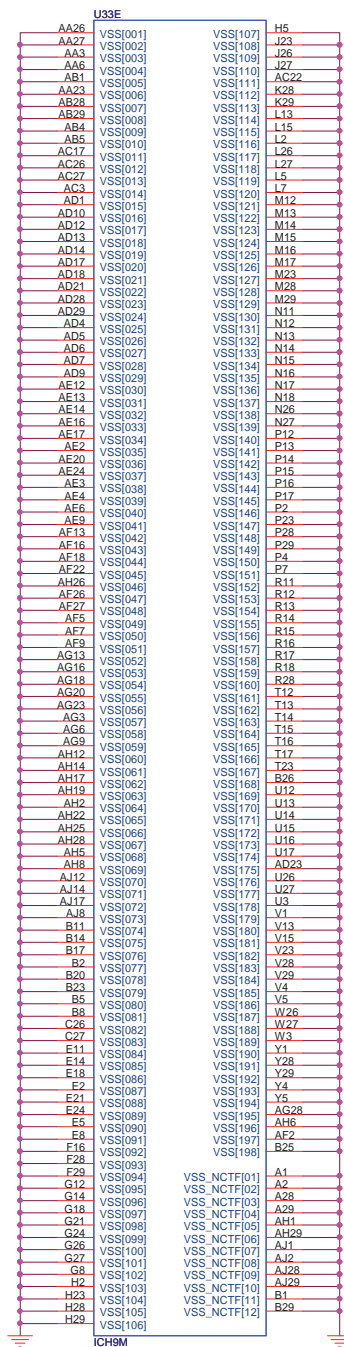





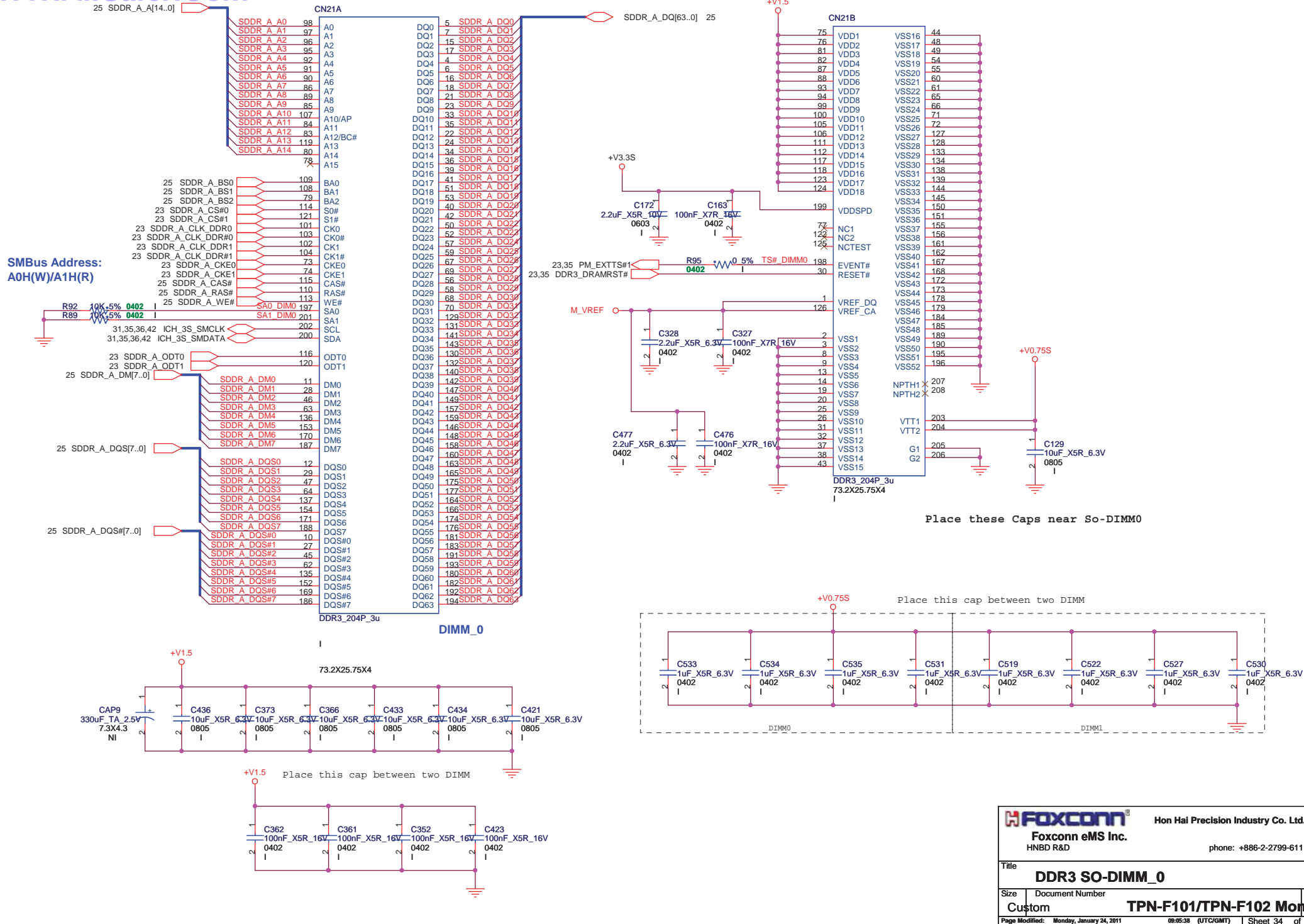








		Hon Hai Precision Industry Co. Ltd.	
Foxconn eMS Inc.		HNBD R&D	
		phone: +886-2-2799-6111	
Title			
ICH9-M( GND) 5/5			
Size	Document Number		Rev
Custom	TPN-F101/TPN-F102 Montevina pl		
Page Modified: Monday, January 24, 2011 08:43:32 (UTC/GMT) Sheet 33 of 46			



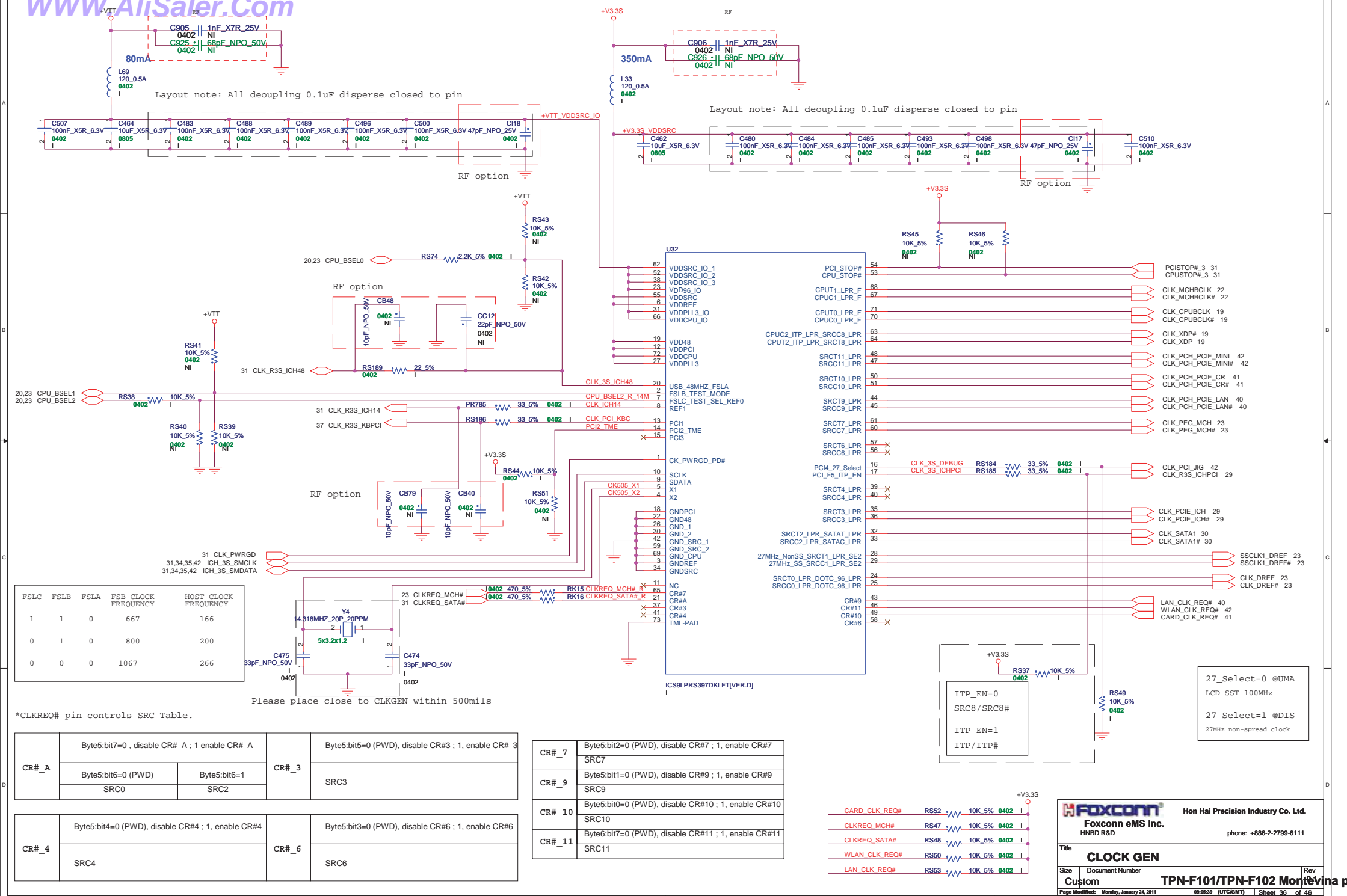
**FOXCONN** Hon Hai Precision Industry Co. Ltd.  
Foxconn eMS Inc.  
HNBD R&D phone: +886-2-2799-6111

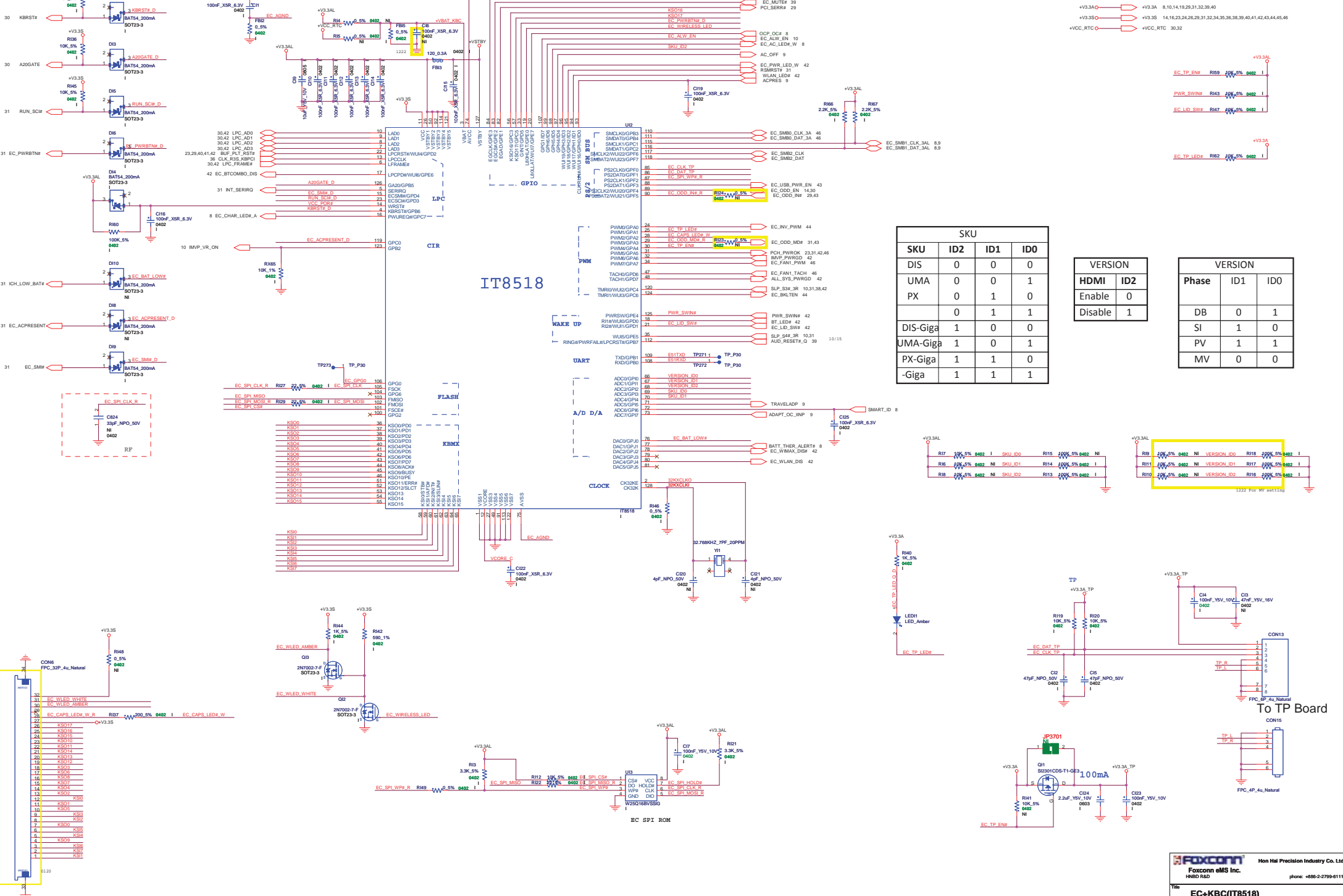
**Title** **DDR3 SO-DIMM\_0**

Size	Document Number	Rev
Custom	TPN-F101/TPN-F102 Montevina	

Page Modified: Monday, January 24, 2011 09:05:38 (UTC/GMT) Sheet 34 of 46



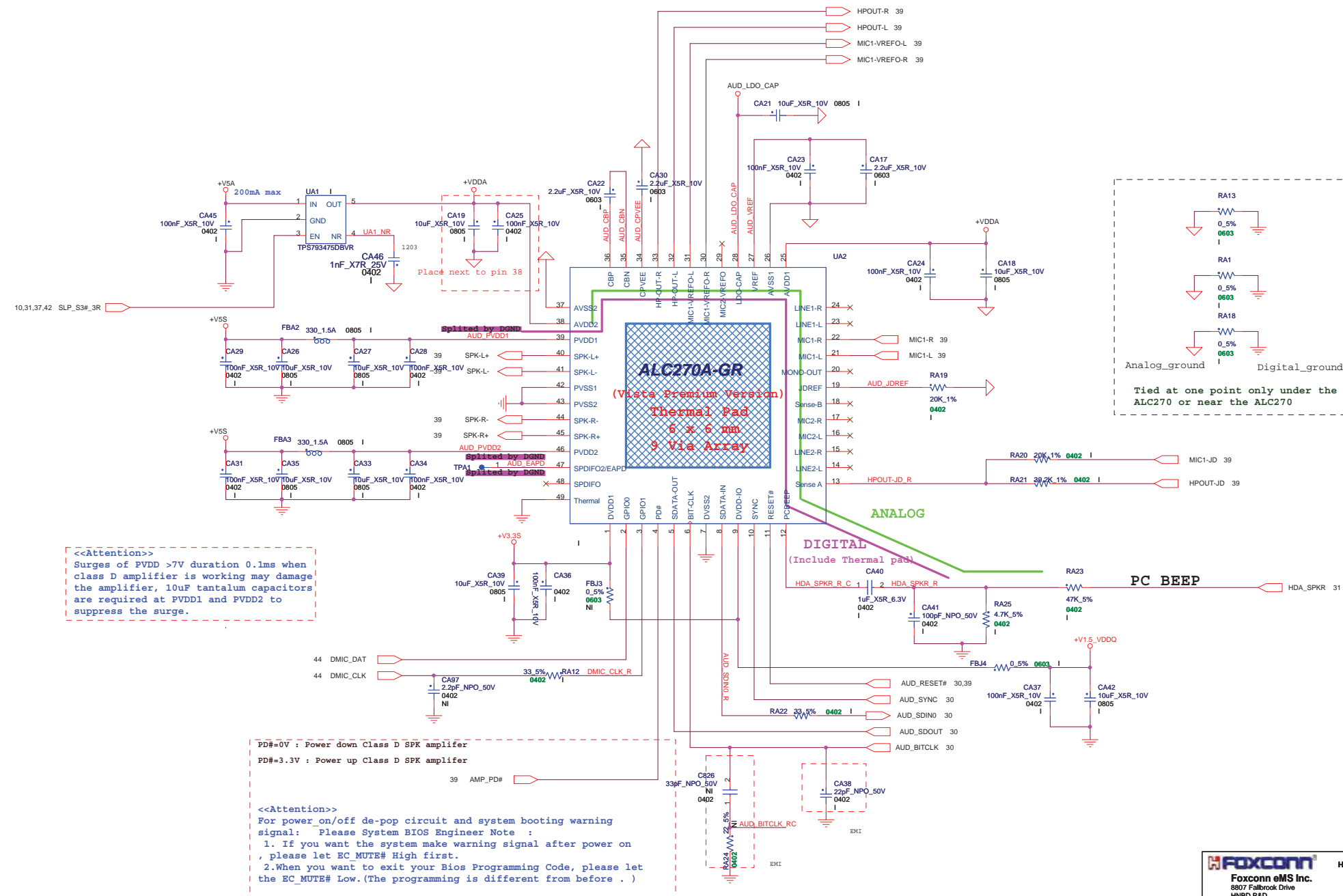


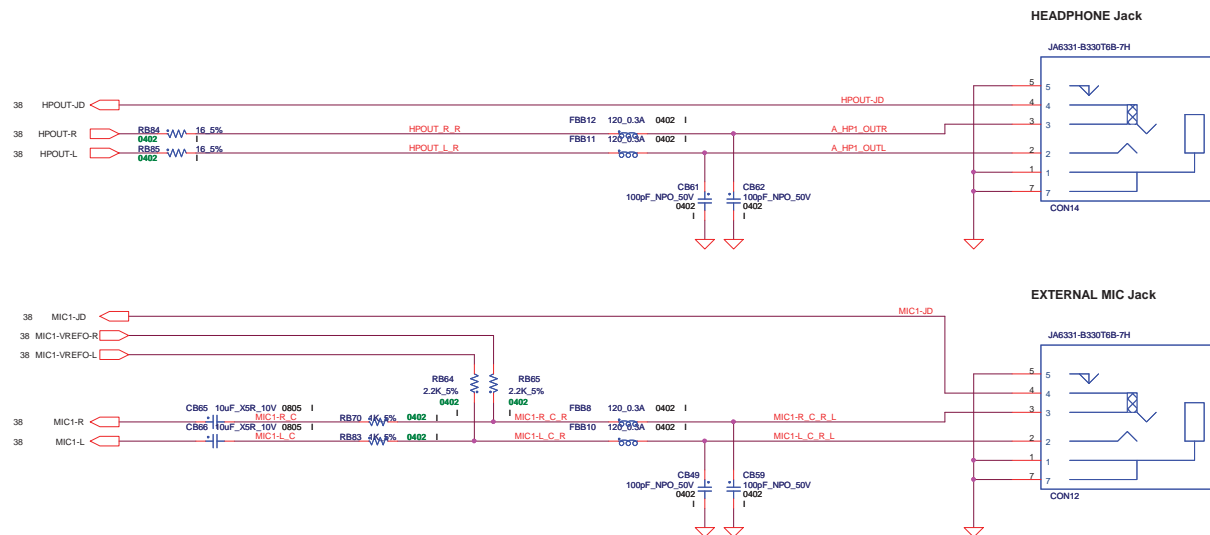
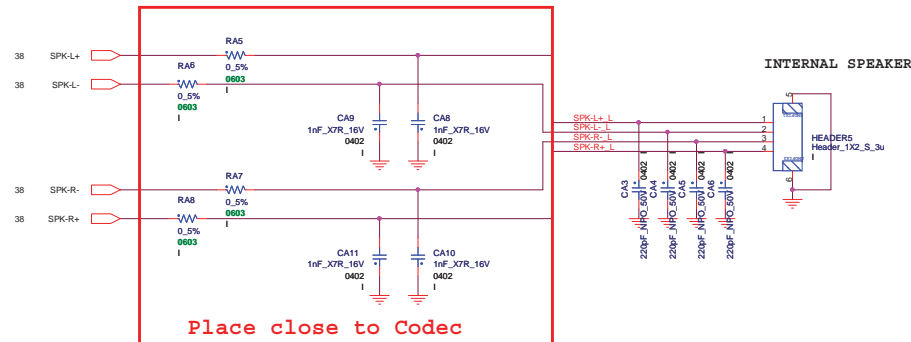
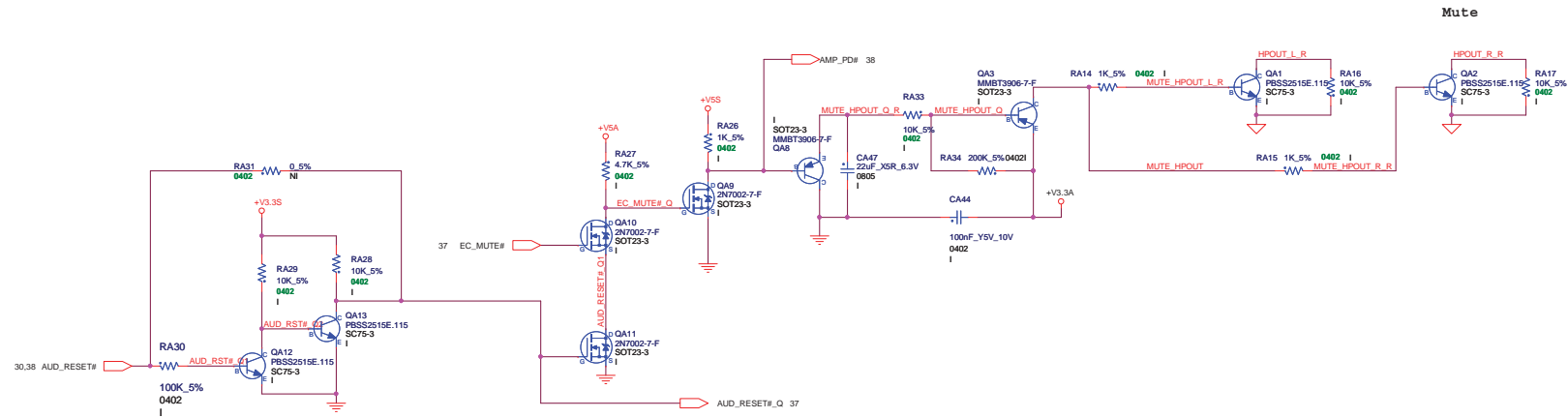


SKU			
SKU	ID2	ID1	ID0
DIS	0	0	0
UMA	0	0	1
PX	0	1	0
DIS-Giga	1	0	0
UMA-Giga	1	0	1
PX-Giga	1	1	0
-Giga	1	1	1

VERSION	
HDMI	ID2
Enable	0
Disable	1

VERSION		
Phase	ID1	ID0
DB	0	1
SI	1	0
PV	1	1
MV	0	0



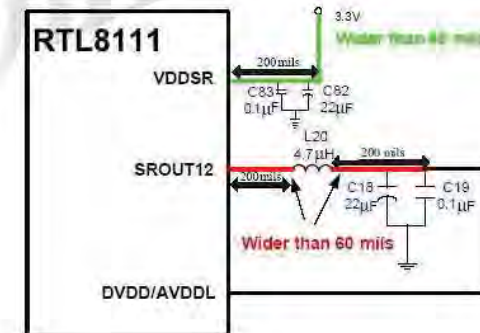






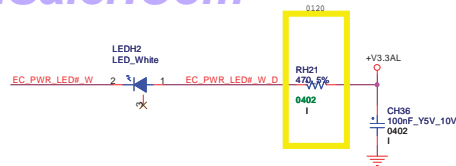
- The input 3.3V power trace connected to the VDDSR pin should be wider than 40mils.
- The bulk de-coupling capacitors (C82 and C83) should be placed within 200mils (0.5cm) of the VDDSR pin to prevent input voltage overshoot.
- The output power trace out of the SROUT12 pin should be wider than 60mils.
- Keep L20 within 200mils (0.5cm) of the SROUT12 pin.
- Keep C18 and C19 within 200mils (0.5cm) of L20 to ensure stable output power and better power efficiency.
- Both C18 and C82 are strongly recommended to be ceramic capacitors.

*Note: Violation of the above rules will damage the IC.*



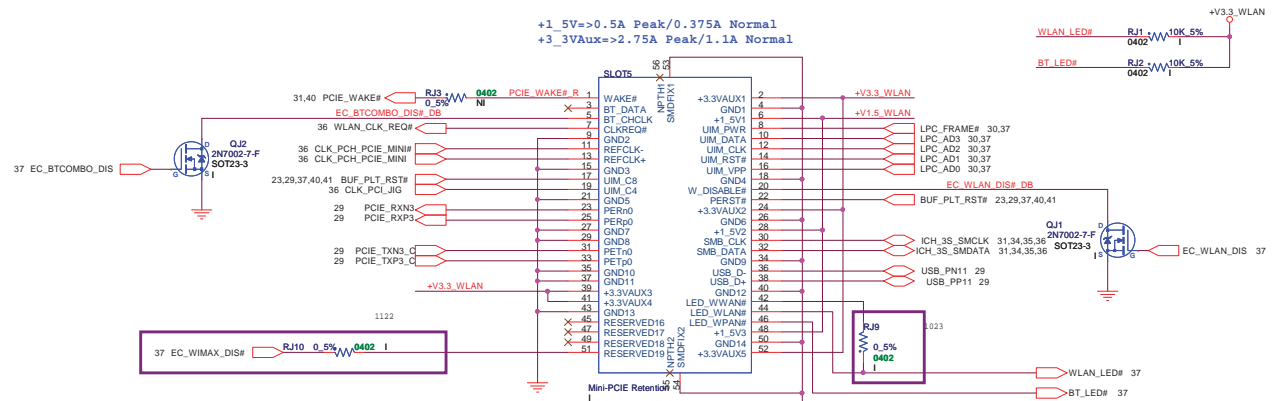
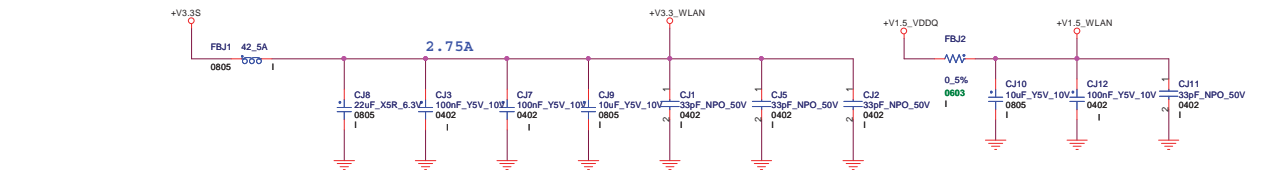
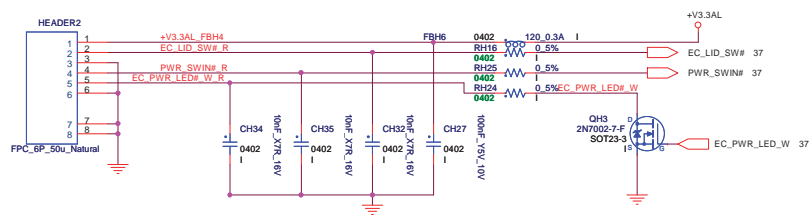




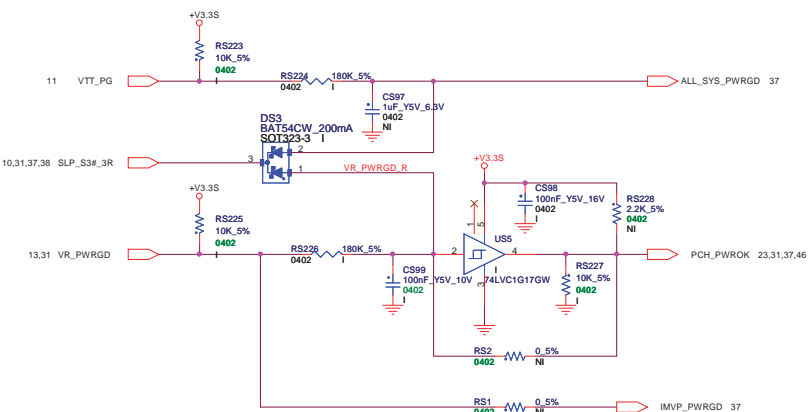


PWR LED

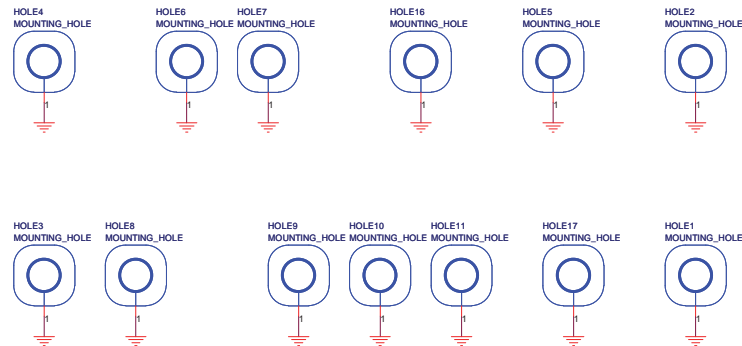
PWR Board CONN.



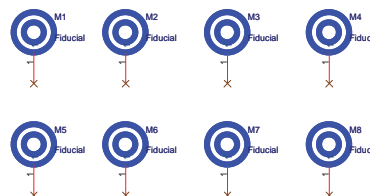
Half Mini Card for WLAN



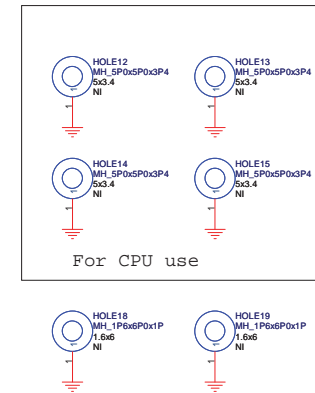
SEQUENCE CIRCUIT

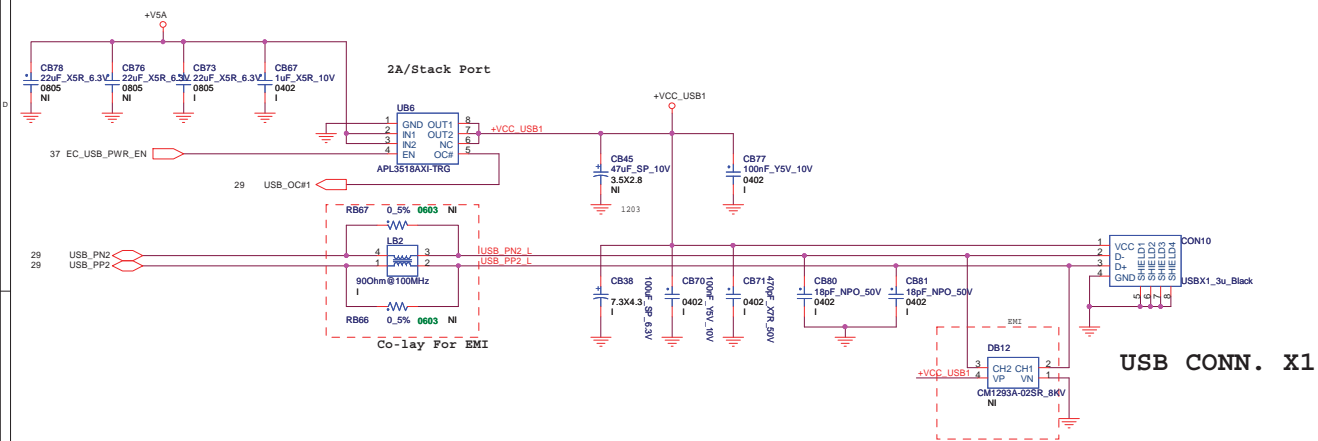


Mounting HOLE

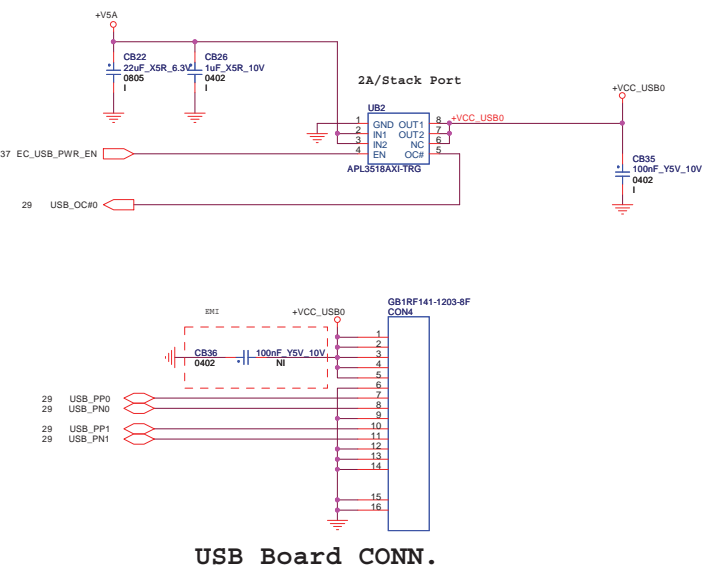


Fiducial Mark



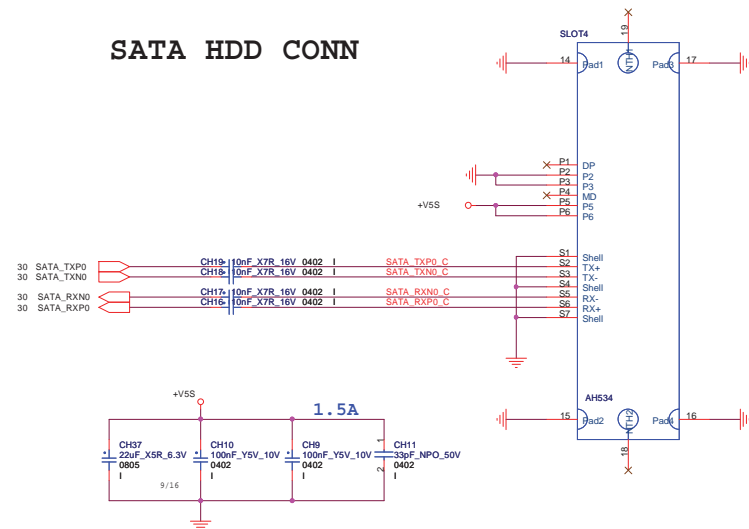


USB CONN. X1

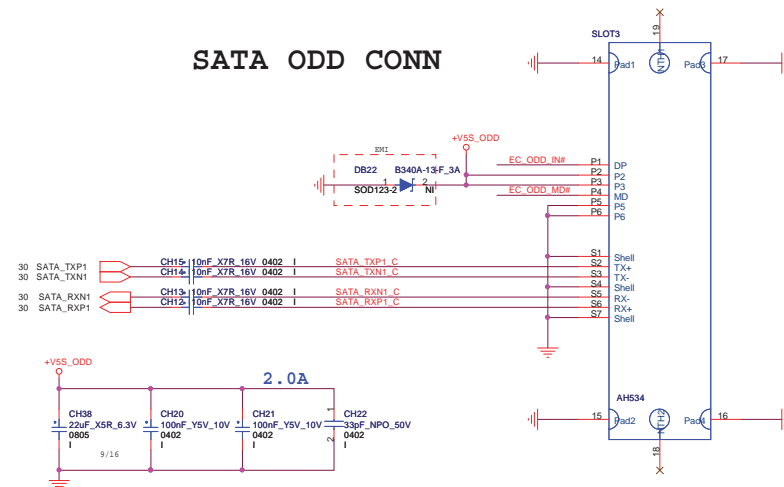


USB Board CONN.

SATA HDD CONN

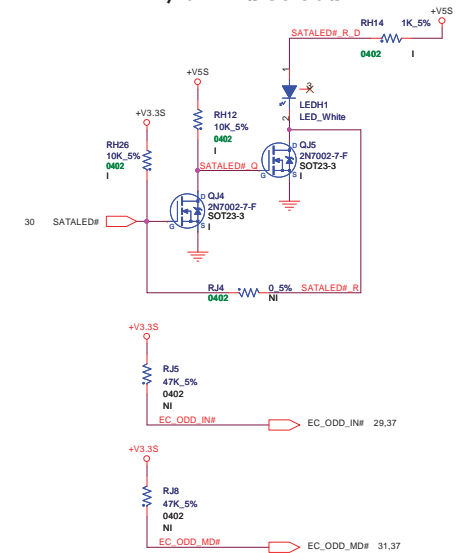


SATA ODD CONN

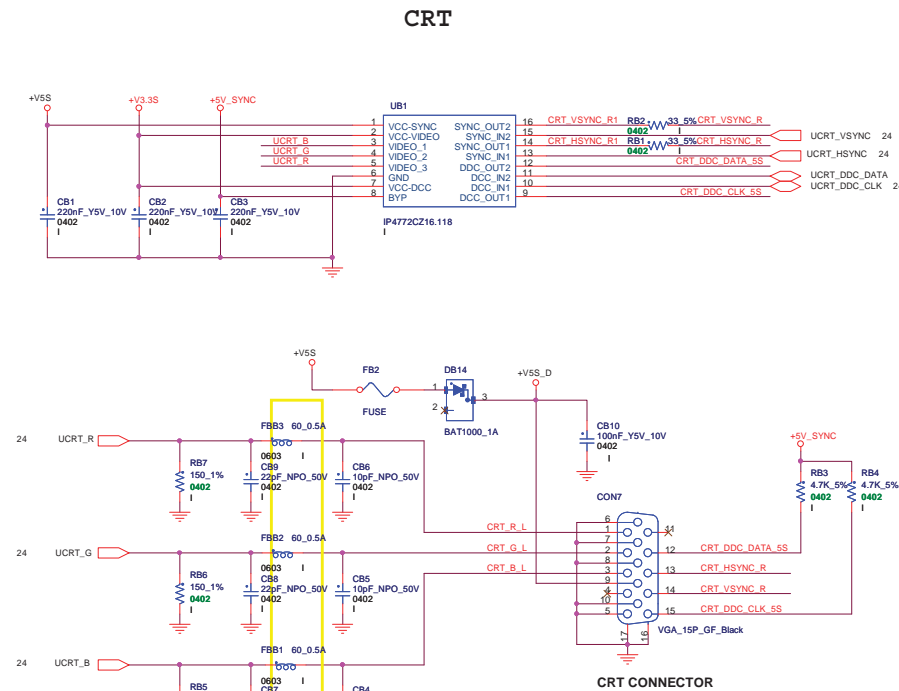


Power pin current  
max. 1300 mA (less 2ms)

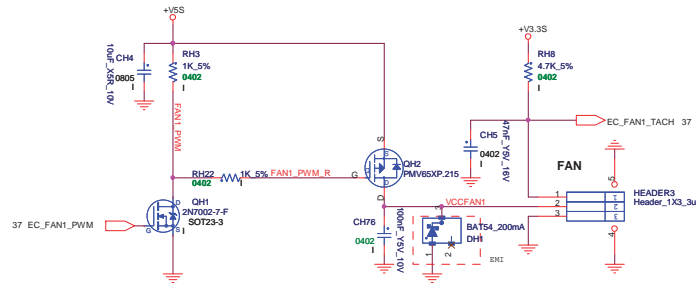
HDD/ODD Status LED



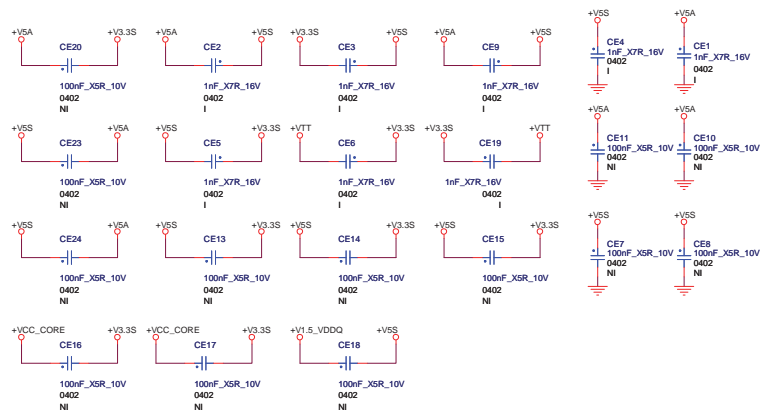
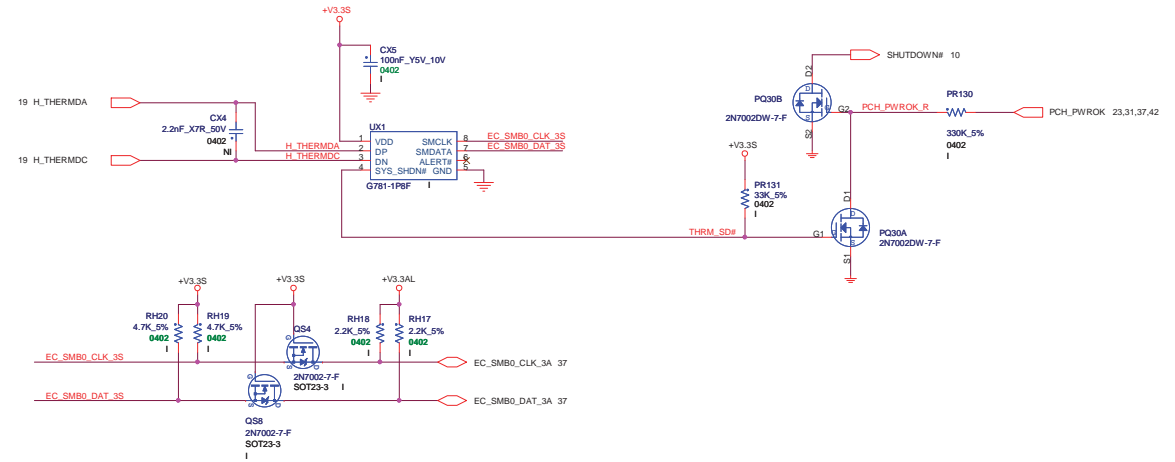




FAN



## THERMAL SENSOR



stitch cap

### RF Solution